Pulsed Power Engineering: Basic Topologies 1

Pulsed Power Engineering
Michigan State University
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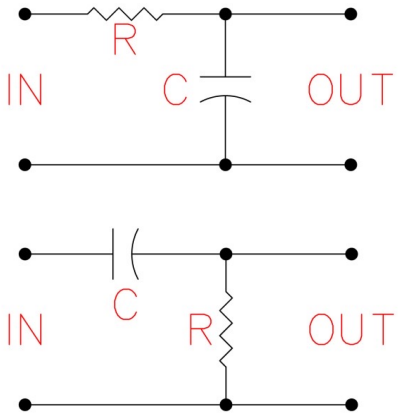
Basic Topologies I

- Basic circuits
- Charging circuits
- Electrical Safety
- Diagnostics
- Grounding and shielding
- Controls

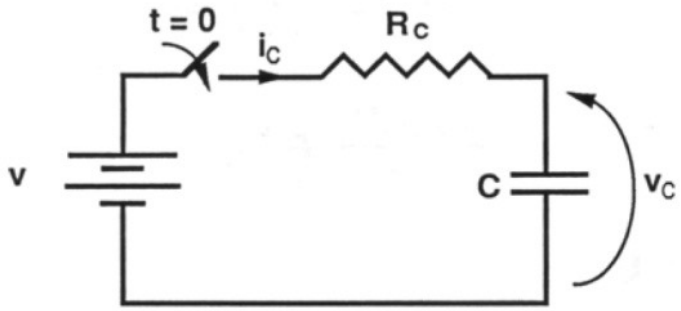
- Basic Topologies II (Class 6)
- Hard tube
- Line-type
  - Transmission line
  - Blumlein
  - Pulse forming network

Basic Circuits: RC

- Capacitor charging
- Capacitor discharging
- Passive integration – low-pass filter
  - $\tau << RC$: integrates signal, $V_{OUT} = (1/RC) \int V_{IN}\, dt$
  - $\tau >> RC$: low pass, $V_{OUT} = V_{IN}$
- Passive differentiation – high-pass filter
  - $\tau >> RC$: differentiates signal, $V_{OUT} = (RC)\, dV_{IN}/dt$
  - $\tau << RC$: high pass, $V_{OUT} = V_{IN}$
- Resistive charging of capacitors



RC Charge Voltage



Natural response

$v/R+C(dv/dt)=0$

$\int^{v} dv/v = \int_0^t (-1/R_C C)\, dt$

$v_C=V_0 \exp(-t/R_C C)$

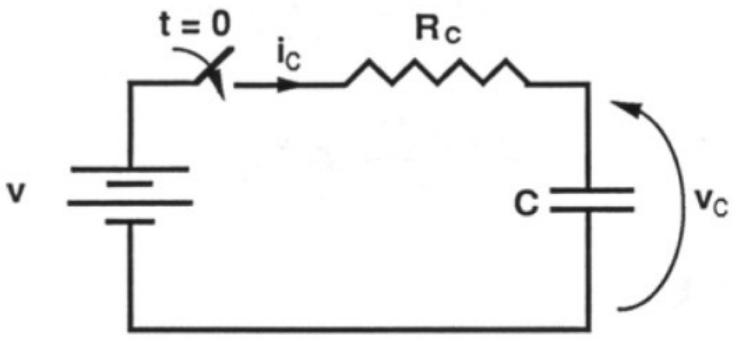
Forced response

$v_C = V_0$

Complete response

$v_C = V_0 - V_0 \exp(-t/R_C C)$

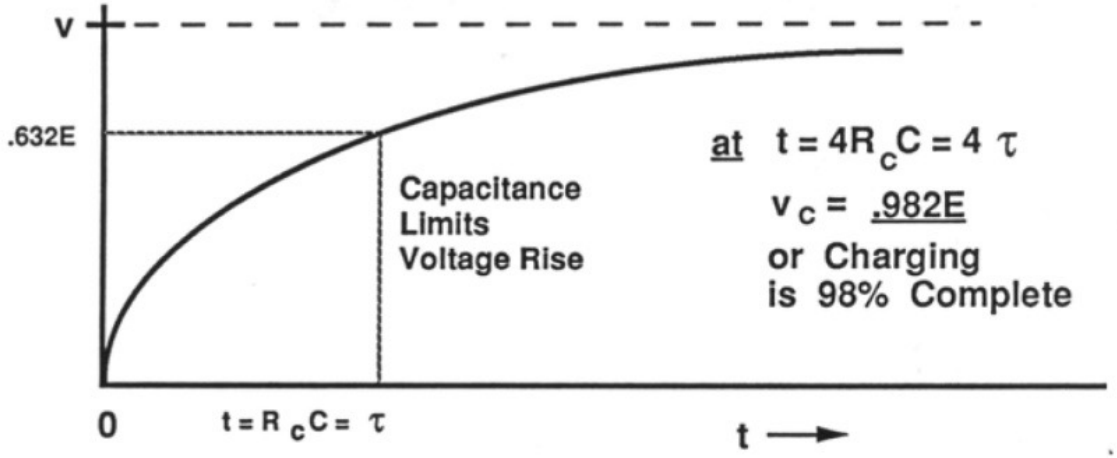
RC Charge Voltage



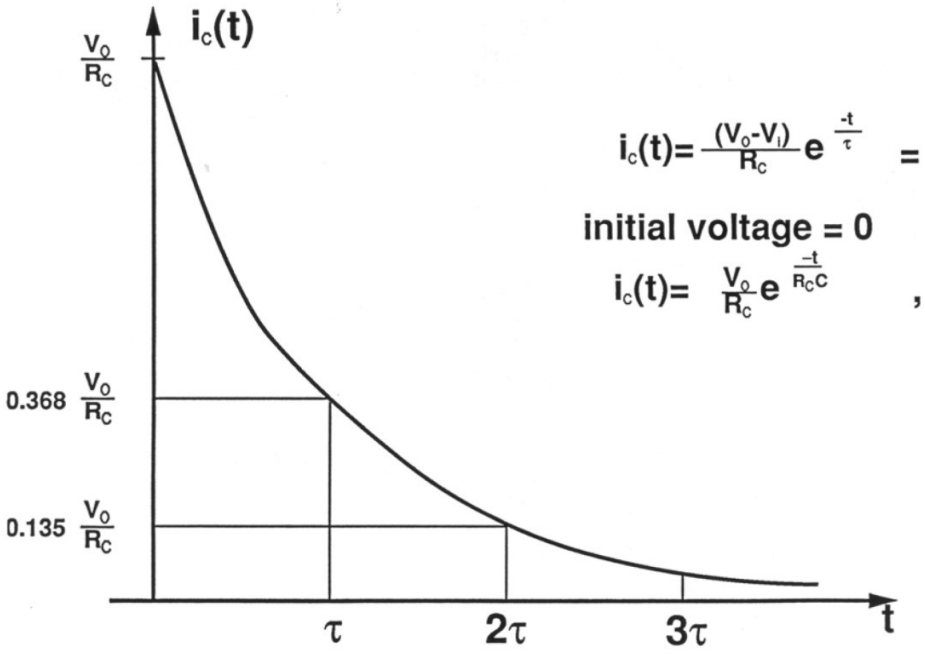
$$v_C = \frac{1}{C}\int i_C\, dt$$

$$v_C = \frac{1}{C}\int_0^t \frac{v}{R_C} e^{-\frac{t}{R_C C}} dt$$

$$= v\left(1 - e^{-\frac{t}{R_C C}}\right)$$



RC Charge Current



$$i_c(t)=\frac{(V_0-V_i)}{R_c}e^{\frac{-t}{\tau}} = \frac{(V_0-V_i)}{R_c}e^{\frac{-t}{R_cC}}$$

initial voltage = 0

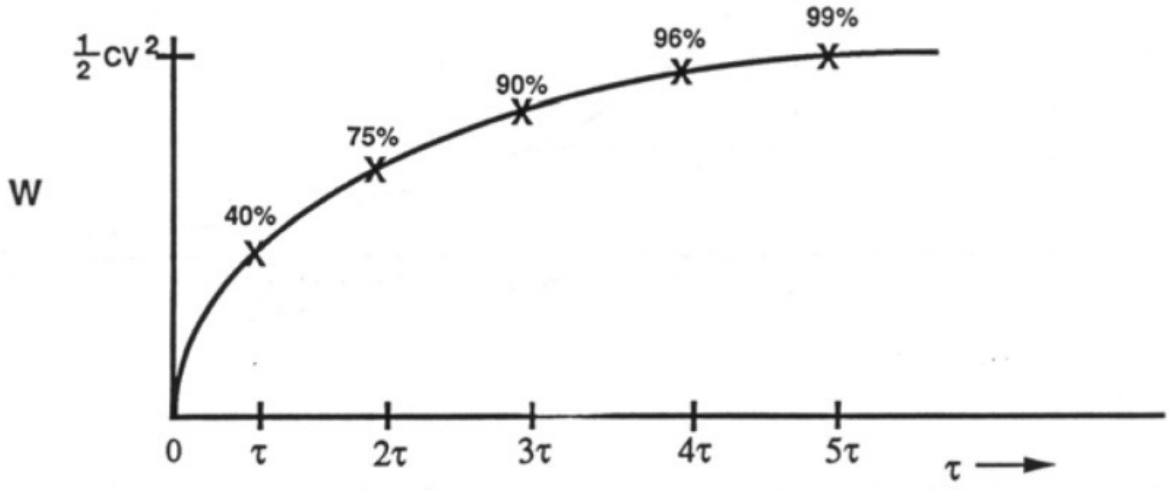
$$i_c(t)=\frac{V_0}{R_c}e^{\frac{-t}{R_cC}}, \quad \tau=R_cC$$

RC Charge Energy

Energy Stored?

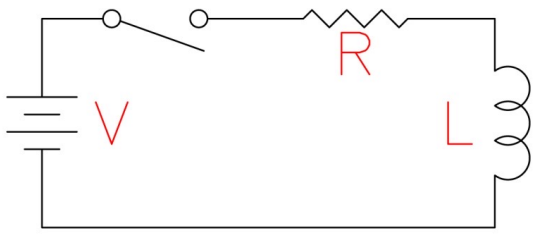
$$W = \int p\,dt = \int_0^t ei\,dt \;,\; i = C\frac{dv}{dt}$$

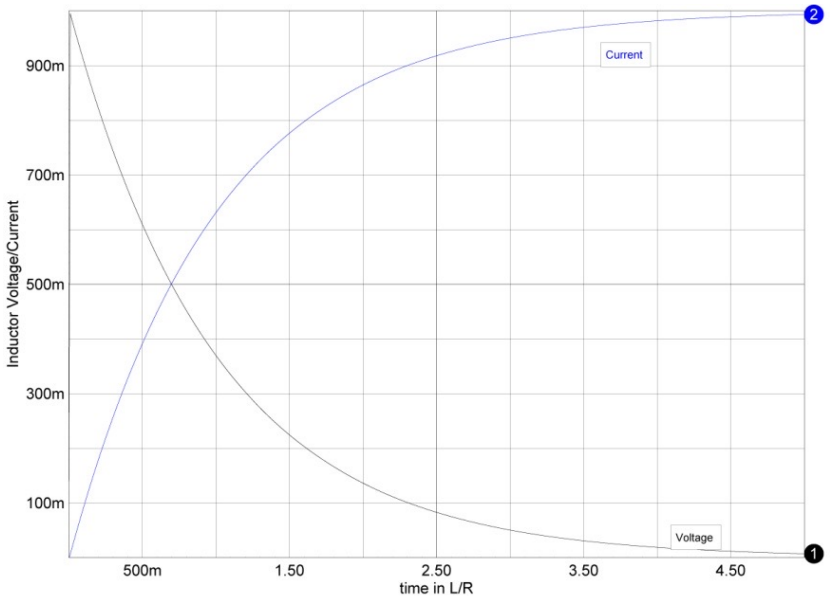
$$\Rightarrow \frac{1}{2}CV^2$$



LR Circuit: Inductive Risetime Limit

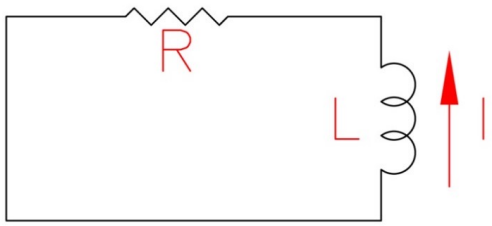
- At t=0, close switch and apply V=1 to LR circuit
- Inductance limits di/dt
- Reach 90% of equilibrium current V/R, in ~2.2 L/R

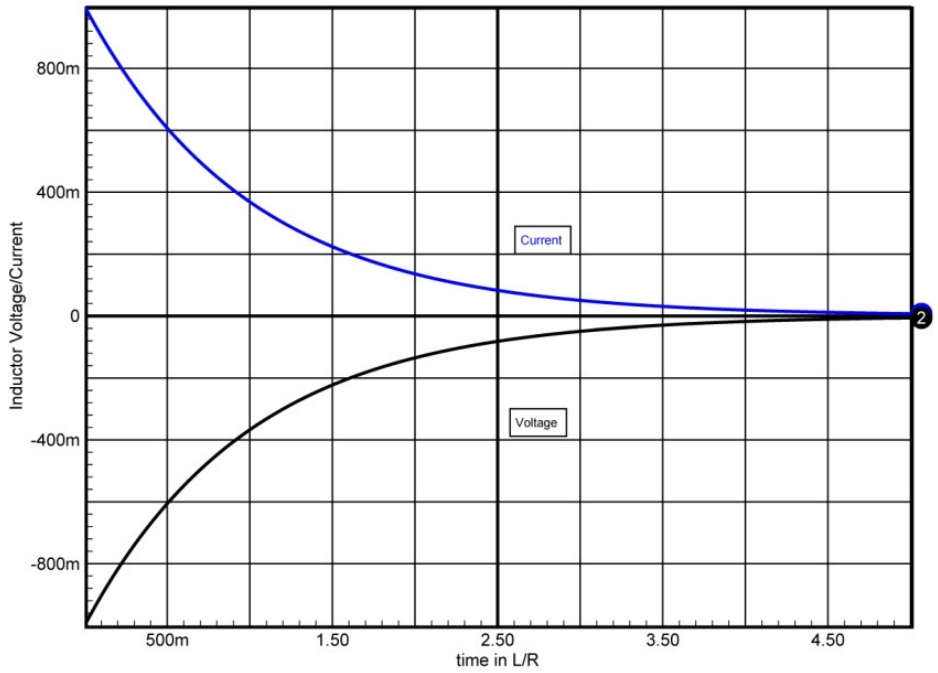




LR Circuit: Decay of Inductive Current

- At t=0, current I=1 flowing in LR circuit
- Fall to 10% of initial current in ~2.2 L/R





LRC Circuit

- Generally applicable to a wide number of circuits and sub-circuits found in pulsed power systems
- Presented in the more general form of CLRC (after NSRC formulary)
  - Limit $C_1 \rightarrow \infty$, reduces to familiar LRC with power supply
  - Limit $C_2 \rightarrow \infty$ (short), reduces to familiar LRC
  - Limit $R \rightarrow 0$, reduces to ideal CLC energy transfer
  - Limit $L \rightarrow 0$, reduces to RC

CLRC Circuit Definitions

$$\tau = \frac{L}{R}$$ 1/2τ is Neper frequency (α)

$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2}$$

$$\omega_o = \frac{1}{\sqrt{LC_{eq}}}$$ Resonant frequency

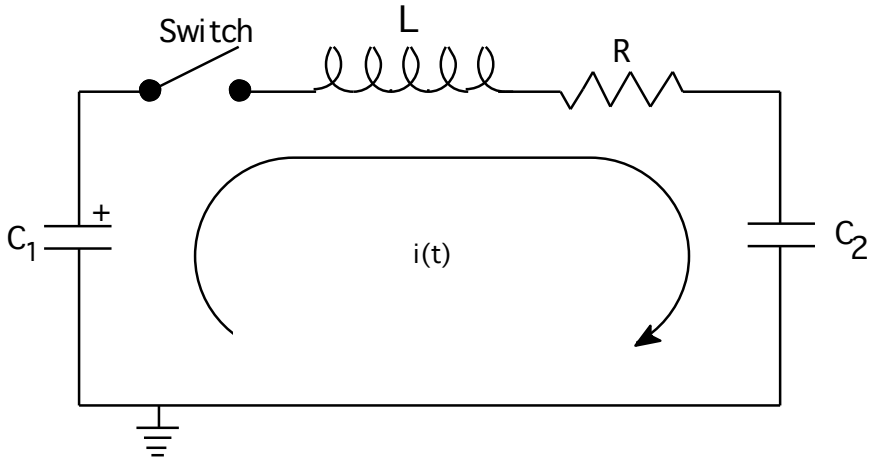
$$\omega^2 = ABS\left(\omega_o^2 - \left(\frac{1}{2\tau}\right)^2\right) = \beta$$ Natural frequency

$$Z_0 = \sqrt{\frac{L}{C_{eq}}}$$

$$Q = \frac{Z_0}{R} =$$ (Circuit Quality Factor)

$V_0 = initial\ \ charge\ \ voltage\ \ on\ \ C_1$

$0 = initial\ \ charge\ \ voltage\ \ on\ \ C_2$



CLRC Circuit General Solutions

$i(t) = A_1\exp(s_1 t) + A_2\exp(s_2 t)$, where

$s_{1,2} = -(1/2\tau) \pm \sqrt{(1/2\tau)^2-\omega_0^2}$

<u>Overdamped</u> ($R > 2(L/C)^{1/2}$, $\beta<0$):

$(1/2\tau) > \omega_0$, $s_{1,2}$ are negative real numbers

$i(t) = A_1\exp(s_1 t) + A_2\exp(s_2 t)$

<u>Critically damped</u> ($R = 2(L/C)^{1/2}$, $\beta=0$):

$(1/2\tau) = \omega_0$, solution to diff. eq. after substitution

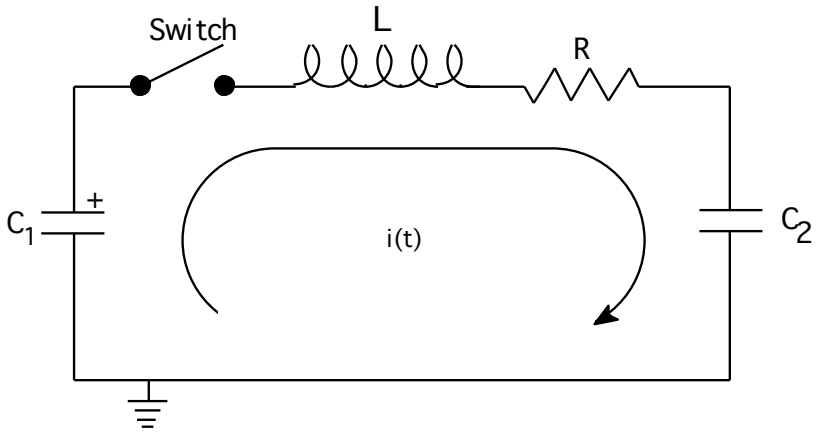
$i(t) = \exp(-t/2\tau)\,(A_1 t - A_2)$

<u>Underdamped</u> ($R < 2(L/C)^{1/2}$, $\beta>0$):

$(1/2\tau) < \omega_0$, $s_{1,2}$ are complex numbers

$i(t) = \exp(-t/2\tau)\,[A_1\exp(j\omega t)+A_2\exp(-j\omega t)]$

$i(t) = \exp(-t/2\tau)\,[B_1\cos(\omega t) + B_2\sin(\omega t)]$



$d^2i(t)/dt^2+(R/L)di(t)/dt+(1/(LC_e))i(t) = 0$

CLRC Behavior: Underdamped limit, R < $2Z_o$

$$i(t) = \frac{V_o}{\omega L} e^{\frac{-t}{2\tau}} \sin \omega t$$

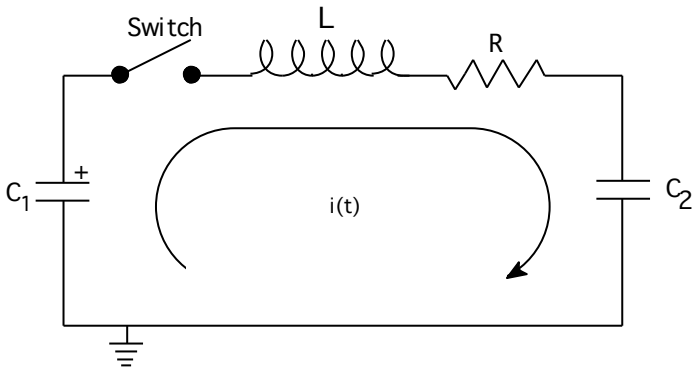
$$V_{C_2}(t) = \frac{V_0 C_1}{C_1 + C_2}\left[1 - e^{\frac{-t}{2\tau}}\left(\frac{1}{2\omega\tau}\sin\omega t - \cos\omega t\right)\right]$$

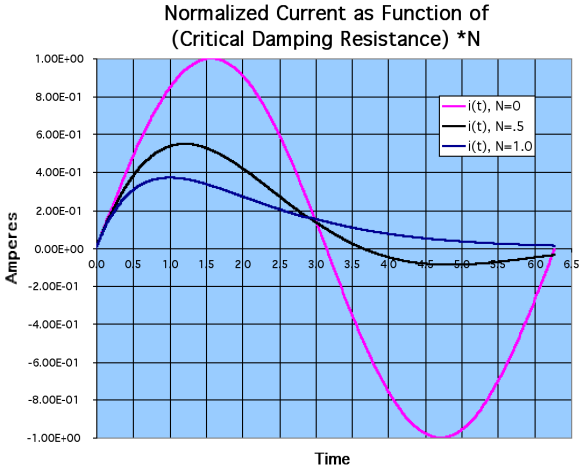
$$i_{peak} @\ t_1 = \frac{1}{\omega}\tan^{-1}(2\omega\tau)$$

$$i_{peak} = \frac{V_0}{\sqrt{\frac{L}{C_{eq}}}} e^{\frac{-t_1}{2\tau}} = \frac{V_0}{Z_0} e^{\frac{-t_1}{2\tau}} \cong \frac{V_0}{Z_0 + 0.8R}$$

$$i(t) = 0\ ;\ V_{C_2}(t) = peak\ @\ \ t_0 = \frac{\pi}{\omega}$$

$$V_{C_2}(t)_{peak} = \frac{V_0 C_1}{C_1 + C_2}\left(1 + e^{\frac{-\pi}{2\omega\tau}}\right)$$





Highly Underdamped, $Z_o/R \rightarrow \infty$: Resonant Energy Transfer

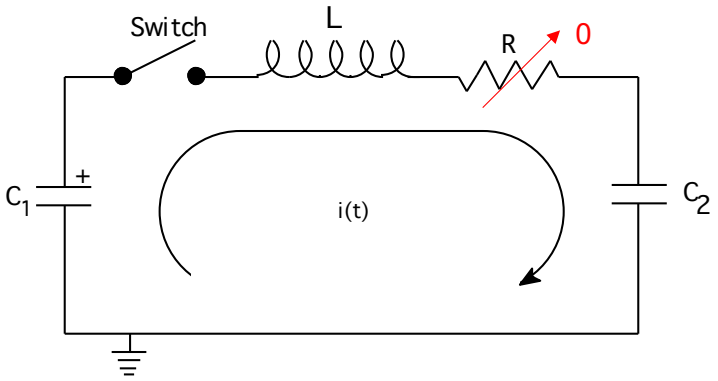
$$i_{peak} = \frac{V_0}{Z_0} \qquad i(t) = (V_0/Z_0)\ sin\ (\omega_0 t)$$

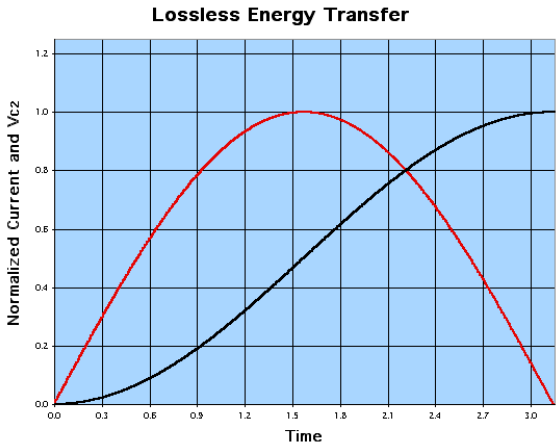
$$i_{peak} @\ t = \frac{\pi}{2\omega_0} = (\pi/2)\sqrt{LC_{eq}}$$

$$V_{C_2}(t) = \frac{V_0 C_1}{C_1 + C_2}\left(1 - \cos(\omega_0 t)\right)$$

$$V_{C_2}(peak) @ t = \frac{\pi}{\omega_0} = \pi\sqrt{LC_{eq}}$$

$$V_{C_2}(peak) = \frac{2V_0 C_1}{C_1 + C_2}$$

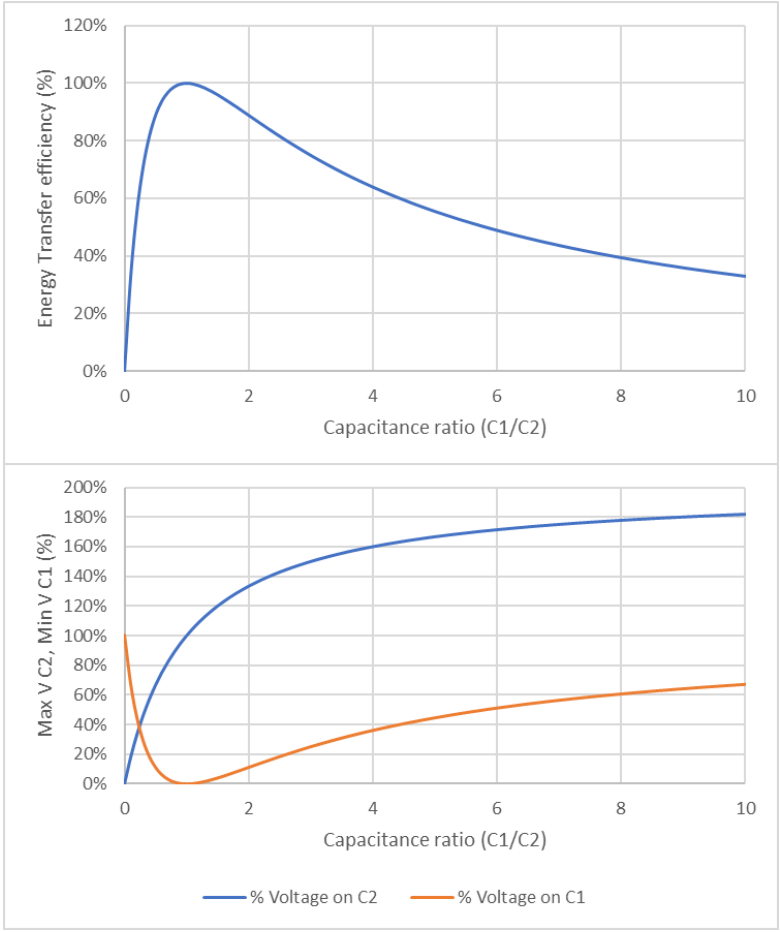




Highly Underdamped: Resonant Energy Transfer (cont.)

- Peak energy transfer efficiency achieved with $C_1 = C_2$
- $\eta = 4C_1C_2/(C_1+C_2)^2$

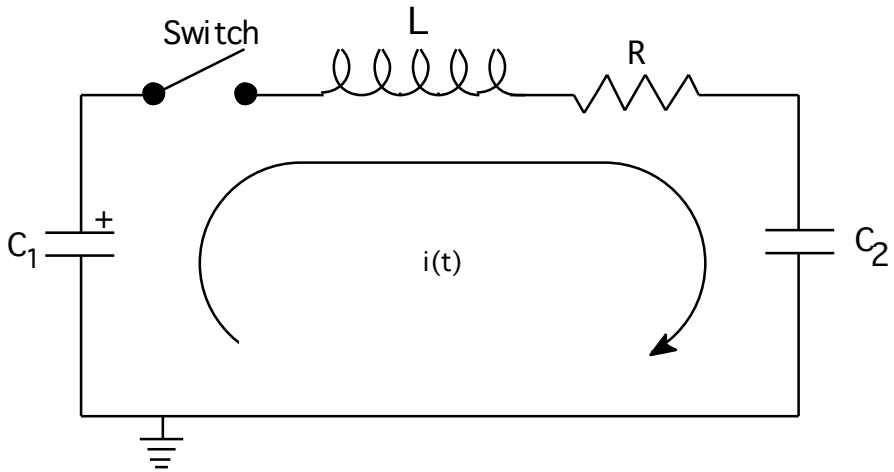
- If $C_1 >> C_2$, the voltage on C_2 will go to twice the voltage on C_1
- $V_{C1,min} = V_0\{1 - 4C_1C_2/(C_1+C_2)^2\}$



CLRC Behavior: Overdamped limit, R >> 2Z_o

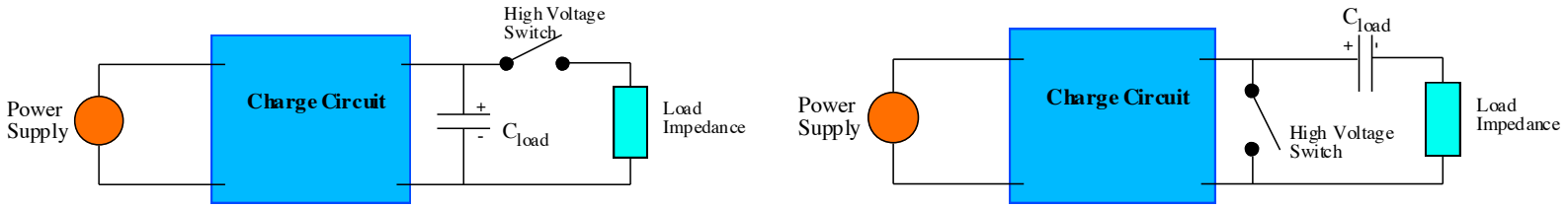
$$i(t) = \frac{V_0\, e^{-\frac{t}{2\tau}}}{2\omega L}\left[e^{\omega t} - e^{-\omega t}\right]$$

$$V_{C_2}(t) = \frac{V_0}{2\omega L C_2}\left[\frac{2\omega}{\omega_o^2} - e^{-\frac{t}{2\tau}}\left(\frac{e^{-\omega t}}{\frac{1}{2\tau}+\omega} + \frac{e^{\omega t}}{\frac{1}{2\tau}-\omega}\right)\right]$$



Charge Circuits - Basics

- The charge circuit is the interface between the power source and the pulse generating circuit and may satisfy the following functions:
  - Ensures that C_{load} is charged to appropriate voltage within the allowable time period.
  - Provides isolation between the power source and the pulse circuit
    - Limit the peak current from the source.
    - Prevent the HV switch from latching into an on state and shorting the power source.
    - May provide voltage gain
    - Isolate the power source from voltage/current transients generated by pulse circuit.

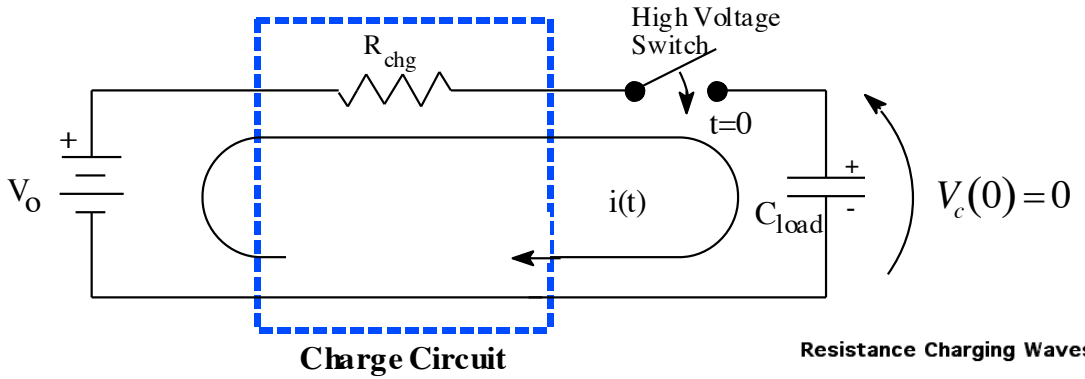


where C_{load} represents the capacitance of a transmission line, PFN, energy storage for a hard-tube circuit, etc.

Charging Topologies

- Resistive charging
- Constant current resistive charging
- Capacitor charging power supplies
- Three phase controller rectifiers
- Inductive charging
  - CLC resonant charge
    - De-Qing

Resistance Charging



Charge Circuit

$$i(t)=\frac{V_o}{R_{chg}}e^{\frac{-t}{R_{chg}C_{Load}}}$$

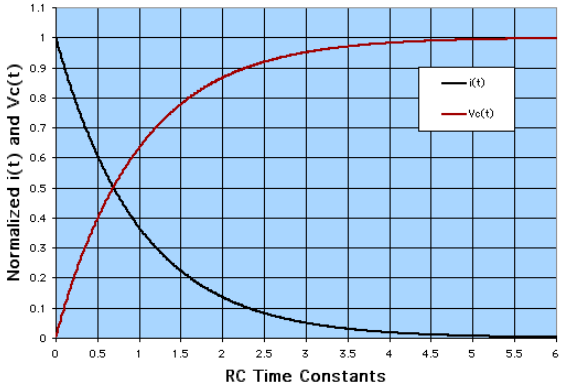
$$V_{C_{Load}}(t)=V_o\left(1-e^{\frac{-t}{R_{chg}C_{Load}}}\right)$$

$$Energy_{Load}\approx\frac{1}{2}C_{Load}V_o^2,\quad t>4R_{chg}C_{Load}$$

$$Energy_{Lost}=\int_0^\infty i^2(t)R_{chg}dt=R_c\int_0^\infty\left(\frac{V_o}{R_c}\right)^2 e^{\frac{-2t}{R_{chg}C_{Load}}}dt$$

$$=\frac{V_o^2}{R_{chg}}\left(-\frac{R_{chg}C_{Load}}{2}\right)e^{\frac{-2t}{R_{chg}C_{Load}}}\Big|_0^\infty=\frac{1}{2}C_{Load}V_o^2$$

Resistance Charging Waveshapes

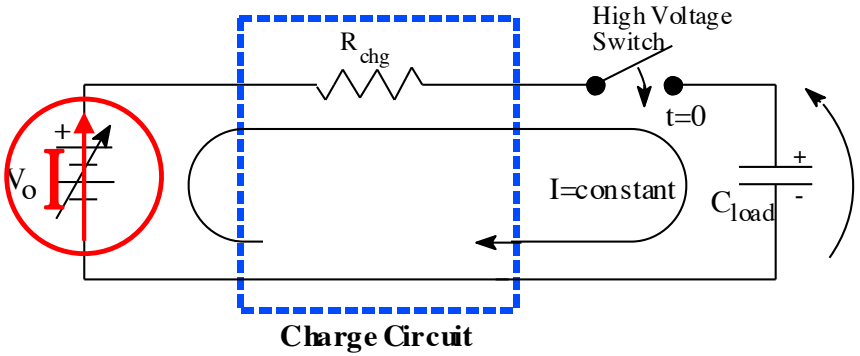


Maximum charging efficiency is 50%
(independent of the value of R_{chg})

Resistance Charging

- Advantages
  - Inexpensive
  - Simple
  - Allows use of low average power, power supply
  - May eliminate the need for a high voltage switch
  - Provides excellent isolation
  - Stable and repeatable
  - Charge accuracy is determined by regulation of power supply
- Disadvantages
  - Inefficient
  - Slow for high energy transfers
  - Requires resistor rated for full charge voltage and, depending on the charge time and energy transferred, a high joule/pulse or average power rating

Constant Current Resistance Charging



$V_c(0) = 0$

$$V_{C_{Load}} = \frac{Q}{C_{Load}} = \frac{IT}{C_{Load}}$$ where T = time for $V_{C_{Load}}$ to approach V_o

$$E_{Lost} = \int_0^T I^2 R_{chg} dt = I^2 R_{chg} T$$

$$E_{Stored} = \frac{1}{2} C_{Load} V_{C_{Load}}^2 = \frac{(IT)^2}{2C_{Load}}$$

$$Efficiency = \frac{E_{Stored}}{E_{Stored} + E_{Lost}} = \frac{T}{T + 2R_{chg}C_{Load}}$$

Efficiency approaches 100% as $T >> 2R_{chg}C_{Load}$

Efficiency = 71% for $T = 5R_{chg}C_{Load}$

Constant Current Charge

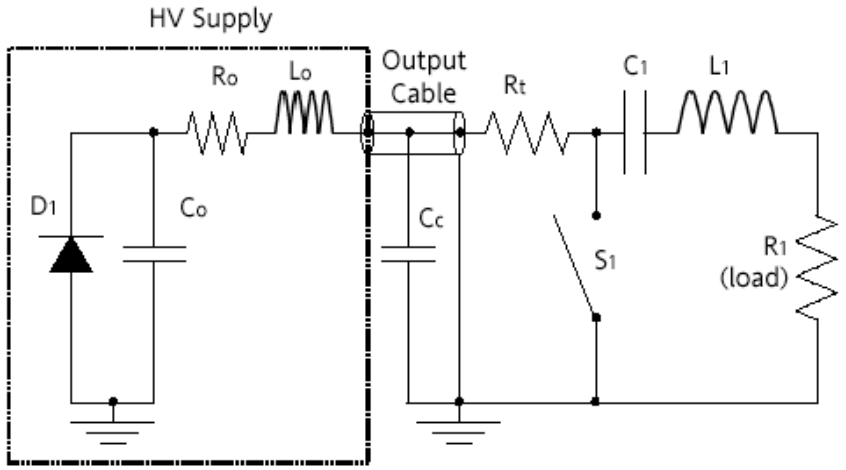
- Advantages
  - Efficient
  - Power and voltage rating on charge resistor is low
  - Can still provide excellent isolation
- Disadvantages
  - More Expensive
    - Constant current power supply generally more expensive than constant voltage
  - Maximum burst rep-rate determined by charge rate

Capacitor Charging Power Supplies

- Positive attributes
  - Efficient (>85%)
  - Low stored energy
  - Stable and accurate (linear to ~1% and with 1% accuracy)
  - Can be operated from DC output to kHz repetition rates
  - Compact (high energy density)
  - Good repeatability (available to <0.1% at rep rates)
  - Output voltage ranges up to 10's of kV and controllable from 0-100% at rated output voltage
  - Charge rate usually specified at Joules/sec
  - Internally protected against open circuits, short circuits, overloads and arcs (usually)
  - Locally or remotely controllable

Capacitor Charging Power Supplies

- Issues
  - Cost ($1-$3 / Peak Watt)
    - You are buying peak power, average power is usually a little less than peak
  - External protection must usually be provided for voltage reversals at load



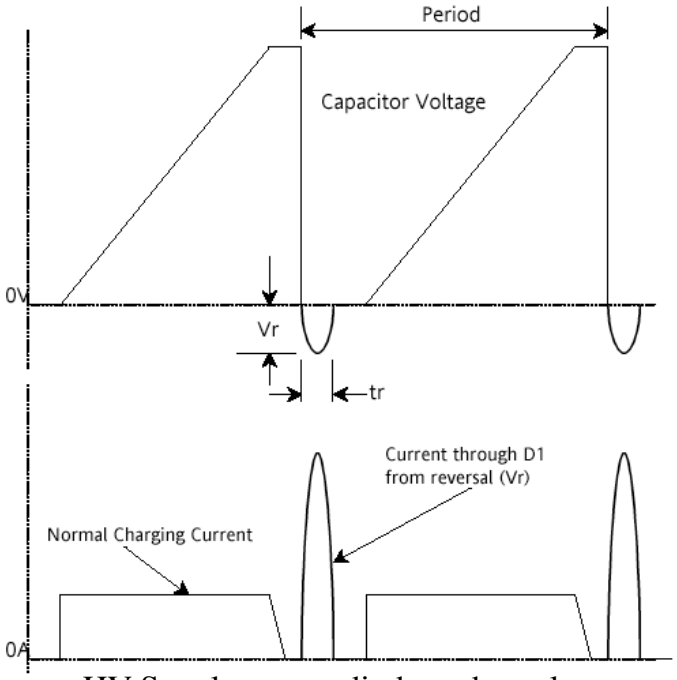
Generalized HV Supply Load Connection

R_t terminates the output cable and prevents the voltage reversal from the closing of switch S_1 from appearing across D_1.

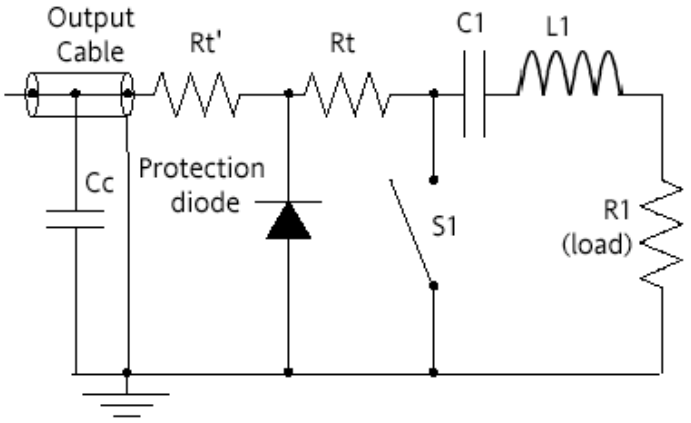
R_o is the internal resistance of the power supply and is usually on the order of a few ohms.

C_o is the internal power supplies internal capacitance and may only be a few hundred pF.

Capacitor Charging Power Supplies



HV Supply output diode under voltage reversal conditions



Voltage Reversal Protection Circuit

The protection diode needs to have:

- a reverse voltage rating that is higher than the circuit operating voltage and the supply operating voltage (with a safety factor)
- a rms current rating higher than seen in the circuit
- a forward voltage drop during conduction that is less than the voltage drop in the power supplies' diodes (if R_t' is not used). If used, Rt' should be selected to limit the current to the supply rated output current or less.

Capacitor Charging Power Supplies

- Useful relationships
  - Output current

    $I_{output} = P_{peak}/V_{rated} = C_{load}V_{chg}/T_c$

  - Peak power

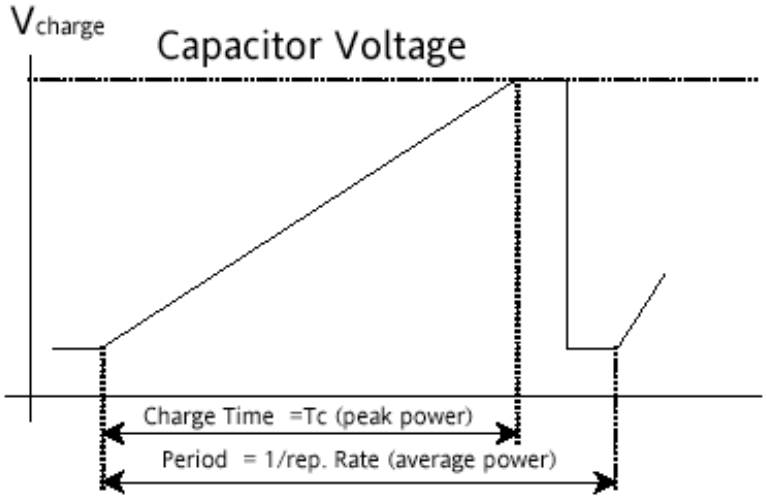
    $P_{peak} = C_{load}V_{chg}V_{rated}/T_c$

  - Charge time

    $T_c = C_{load}V_{chg}V_{rated}/P_{peak}$

  - Maximum repetition rate

    $PRF_{max} = P_{avg}/(C_{load}V_{chg}V_{rated})$

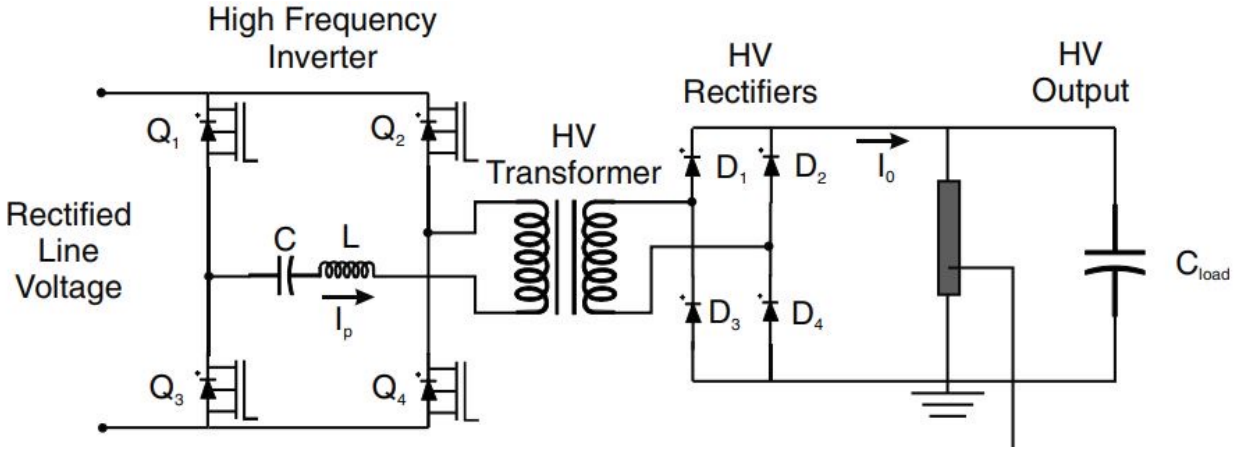


Where:

T_c is the load charge time in seconds
P_{peak} is the unit peak power rating
C_{load} is the load capacitance in Farads
V_{chg} is the load charge voltage in volts
V_{rated} is the power supply rating in volts

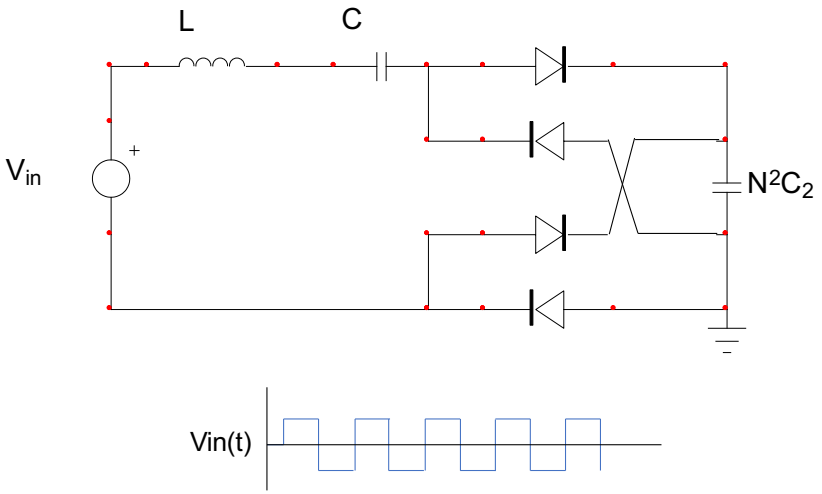
Capacitor Charging Power Supplies

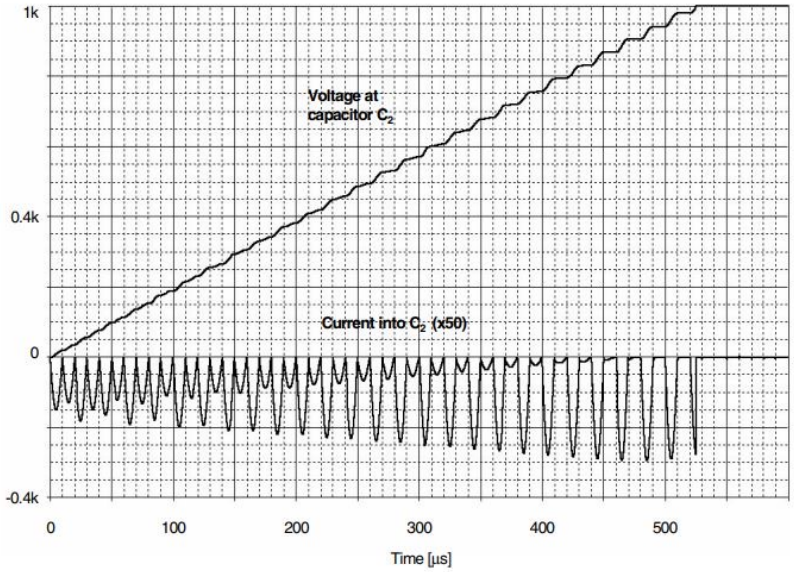
- Switch-mode power supplies (series-resonant converter)
- Constant current on recharge time scales, but little output filtering so high frequency content on the output current
  - May result in increased losses in charge circuit components (e.g. diodes)



Bluhm, H., *Pulsed Power Systems Principles and Applications*, Springer, 2006

Capacitor Charging Power Supplies





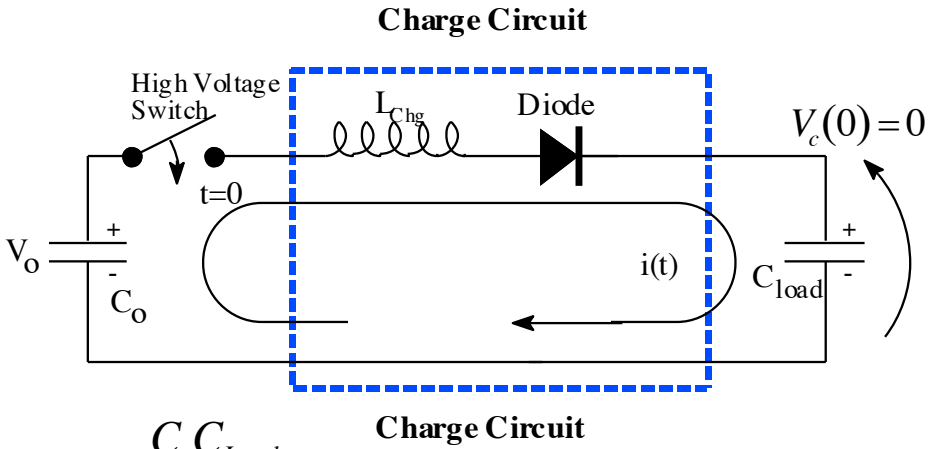
$i(t) = (V_{in}-V_{C2}/N)(C_{eq}/L)^{1/2} \sin(\omega_0 t) \approx (V_{in}-V_{C2}/N)(C/L)^{1/2} \sin(\omega_0 t)$

$N^2C_2 >> C$ so resonance is not affected by the load capacitance

Behaves as a constant current supply

DC Resonant Charge - Capacitor to Capacitor

RLC circuit with diode to block reverse ringing and permit switch recovery



$$i(t)=\frac{V_o}{\sqrt{\frac{L_{chg}}{C_{eq}}}}\sin\left(\frac{t}{\sqrt{L_{chg}C_{eq}}}\right)=\frac{V_o}{Z}\sin\omega t \qquad \text{where} \quad C_{eq}=\frac{C_oC_{Load}}{C_o+C_{Load}}$$

$$\text{At peak voltage}\left(t=\frac{\pi}{\omega}\right): V_{C_{Load}}=2Vo\frac{C_{eq}}{C_{C_{Load}}}$$

$$\text{For } C_o=10C_{Load}: \quad V_{C_{Load}}=\frac{2V_oC_o}{C_o+C_{Load}}=1.82V_o$$

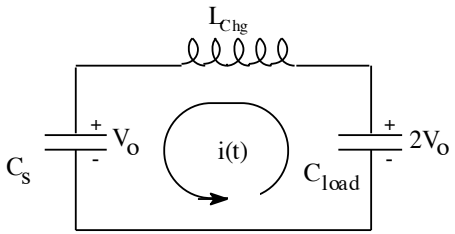
DC Resonant Charge - Capacitor to Capacitor

- Advantages
  - Efficient
  - Voltage gain reduced the PS voltage requirement
  - Easily capable of high repetition rate operation
  - Can operate asynchronously
  - Power supply isn't required to provide large charge current when system is operating at low duty factor
  - Low di/dt requirements on high voltage switch
- Disadvantages
  - Requires a large DC capacitor bank
  - DC capacitor bank needs to be fully recharged between pulses to ensure voltage regulation at the load, unless alternative regulation techniques are employed

Effects of Stray Capacitance

After C_{Load} is charged :

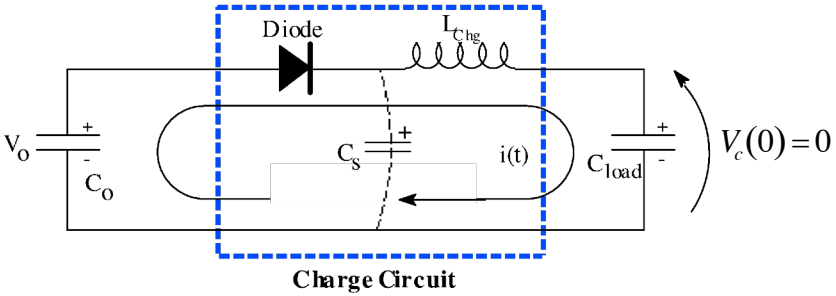
$$V_{C_{Load}} \cong 2V_o \text{ and } V_{C_s} \cong V_o$$



$$i(t) = \frac{V_o}{\sqrt{\frac{L_{chg}}{C_{eq}}}} \sin(\omega t) = \frac{V_o}{Z} \sin \omega t$$

$$V_{C_s} = 2V_o - V_o \cos \omega t$$

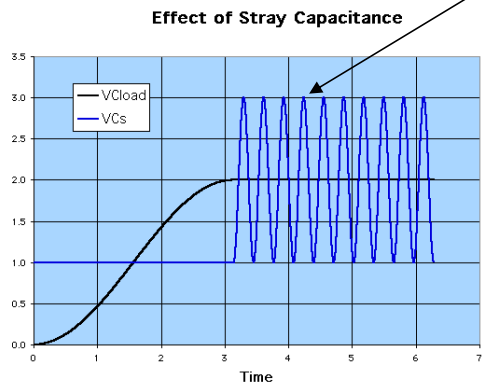
where $C_{eq} = \dfrac{C_s C_{Load}}{C_s + C_{Load}}$ and $\omega = \dfrac{1}{\sqrt{L_{chg} C_{eq}}}$



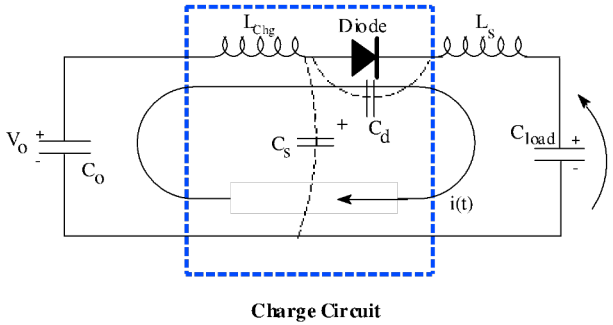
C_s = Stray Capacitance to ground

$C_o >> C_{Load} >> C_s$

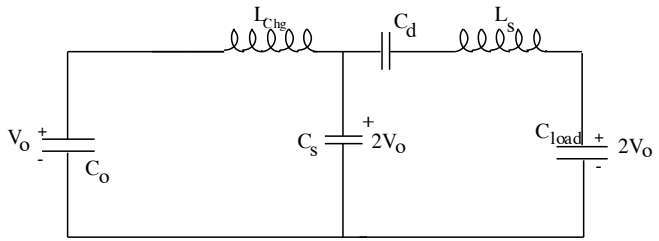
Peak inverse diode voltage >$2V_o$ instead of V_o



Effect of Stray Capacitance



Charge Circuit



C_s - stray capacitance to ground

C_d - stray capacitance across diode stack (includes diode junction capacitance, capacitance between mounting connections, etc.)

L_s- total series inductance between diode and ground

Equivalent Circuit where: $C_o >> C_{Load} >> C_s, C_d$

After C_{Load} is charged:

C_s will ring with C_o and can create large inverse voltage across the diode stack

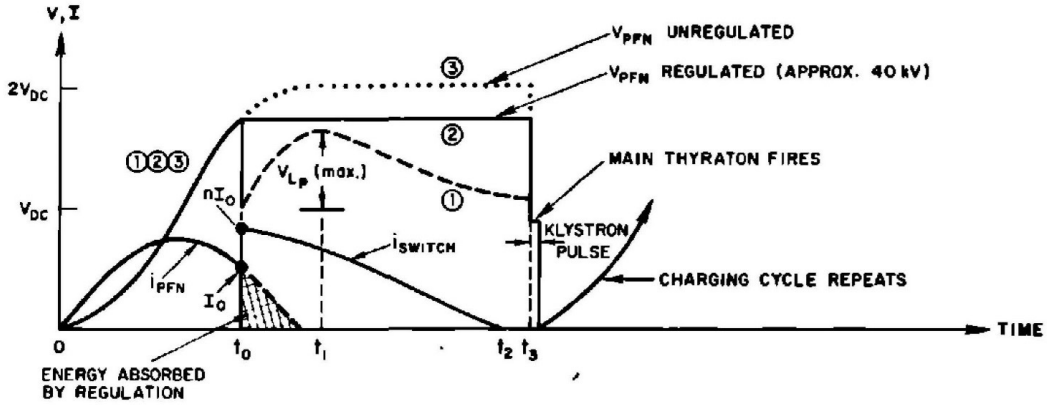
C_{Load} will oscillate with C_d and C_s

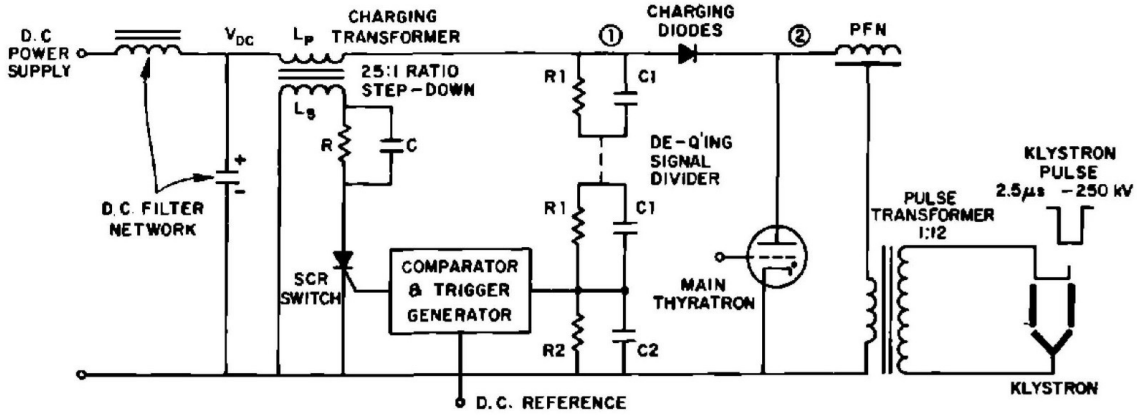
Inductor Snubber and/or Diode Snubber may be required

Inductive Charging Voltage Regulation

- For klystron phase stability, PFN charge voltage regulation may need to be ~10 ppm
- High power supplies usually do not have precise regulation
  - Requires more complicated topologies (over simple rectifier/filter)
  - Increases cost
- Common approach to regulate PFN charge voltage from unregulated source is de-Qing
  - Monitor PFN voltage during charge cycle
  - When PFN reaches final voltage, shunt energy remaining in charge inductor to dummy load

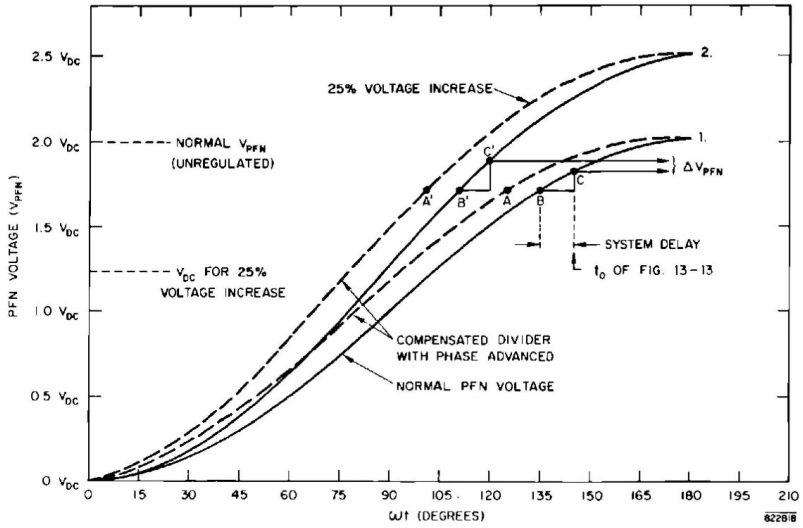
De-Qing


V, I
2V_DC
V_DC
V_PFN UNREGULATED
V_PFN REGULATED (APPROX. 40 kV)
MAIN THYRATON FIRES
V_Lp (max.)
nI_O
i_SWITCH
KLYSTRON PULSE
CHARGING CYCLE REPEATS
i_PFN
I_O
TIME
0
t_0
t_1
t_2 t_3
ENERGY ABSORBED BY REGULATION


D.C POWER SUPPLY
V_DC
L_P
CHARGING TRANSFORMER
25:1 RATIO STEP-DOWN
L_S
R
C
D.C. FILTER NETWORK
SCR SWITCH
COMPARATOR & TRIGGER GENERATOR
CHARGING DIODES
R1
C1
DE-Q'ING SIGNAL DIVIDER
R2
C2
MAIN THYRATON
PFN
PULSE TRANSFORMER 1:12
KLYSTRON PULSE 2.5μs −250 kV
KLYSTRON
D.C. REFERENCE

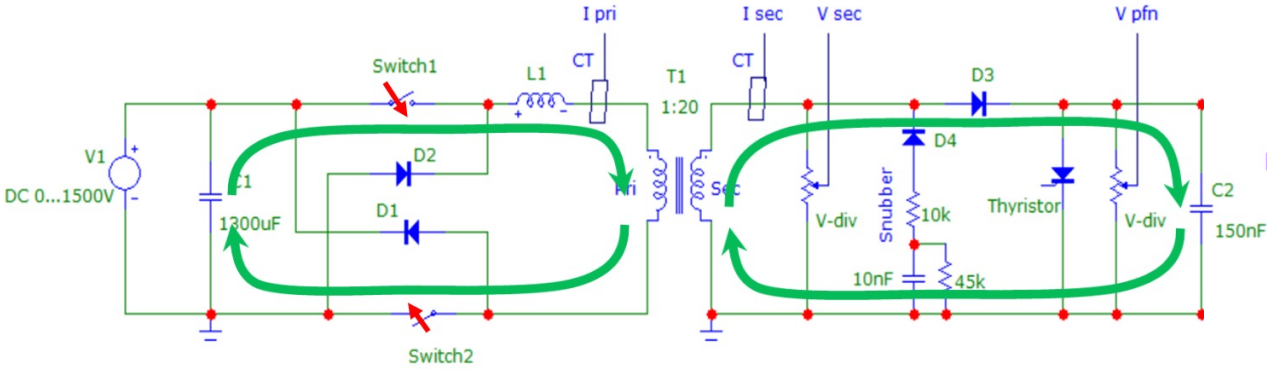
De-Qing Limitation

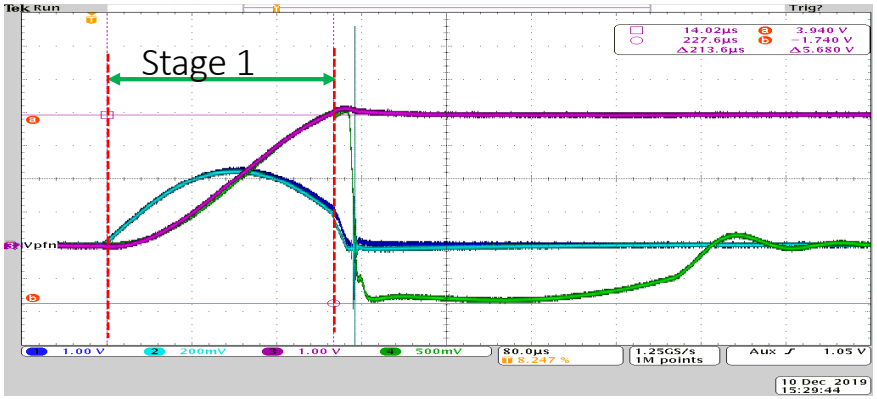
- During the delay between the measurement of the PFN reaching the desired charge voltage and the termination of charging current (system delay), the PFN voltage continues to increase
- When the unregulated source voltage is higher, charging current is increased and the PFN voltage increase during the system delay is increased (ΔV_{PFN})
- This error must be corrected for precise PFN voltage regulation
  - Phase advance on voltage divider
    - Measured signal, V_M, actually higher than PFN voltage, V_{PFN}
    - Ratio of V_M/V_{PFN} is a function of PFN charge rate
    - Compensates delay
    - Used in SLAC 6575
  - Feed forward control loop
    - Measure final PFN voltage
    - Adjust timing if voltage fluctuates
  - Similar regulation accuracy



Alternative to de-Qing

- Traditional resonant charging through transformer in Stage 1



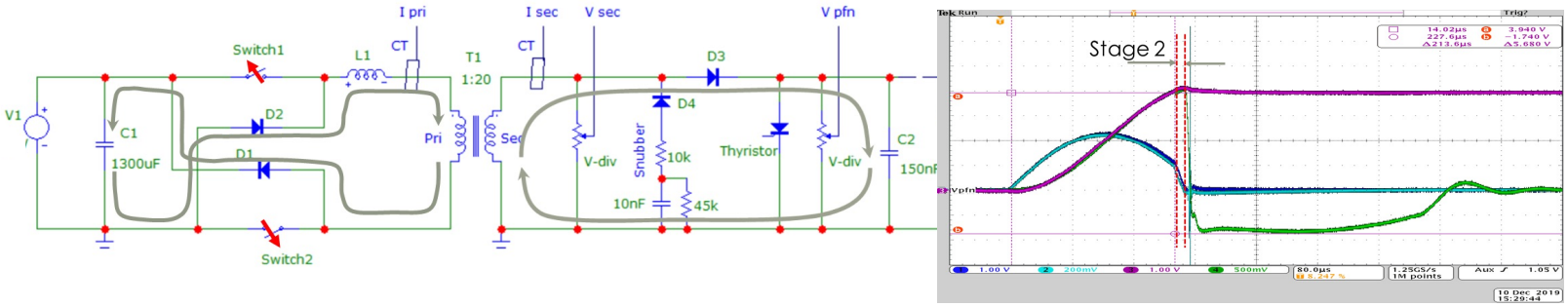


Ch.1: I primary
Ch.2: I secondary
Ch.3: PFN Voltage
Ch.4: Secondary Voltage

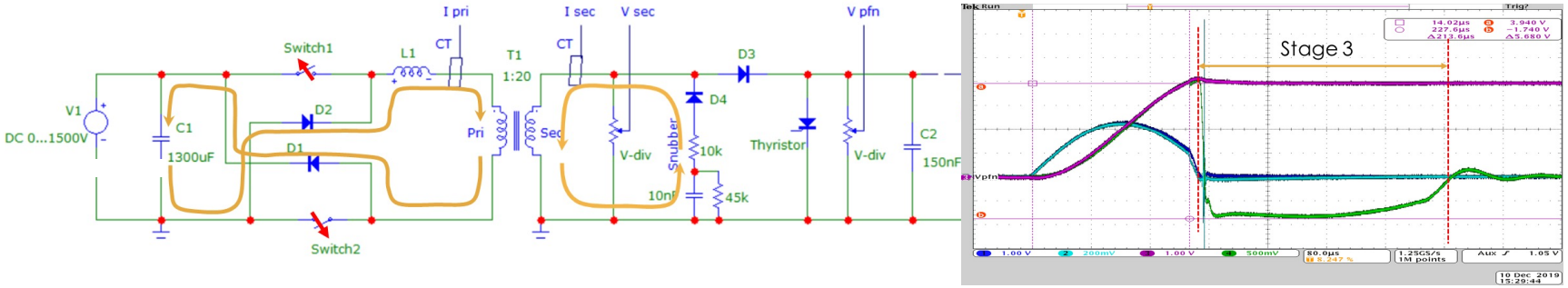
Sathre, R., SNS Extraction Kicker System Mini-Seminar, Feb. 2021.

Alternative to de-Qing

- Energy in primary magnetizing inductance and L1 recovered through D1/D2 after Switch1 and Switch2 open
- Stage 2 freewheels until current in transformer secondary reverses

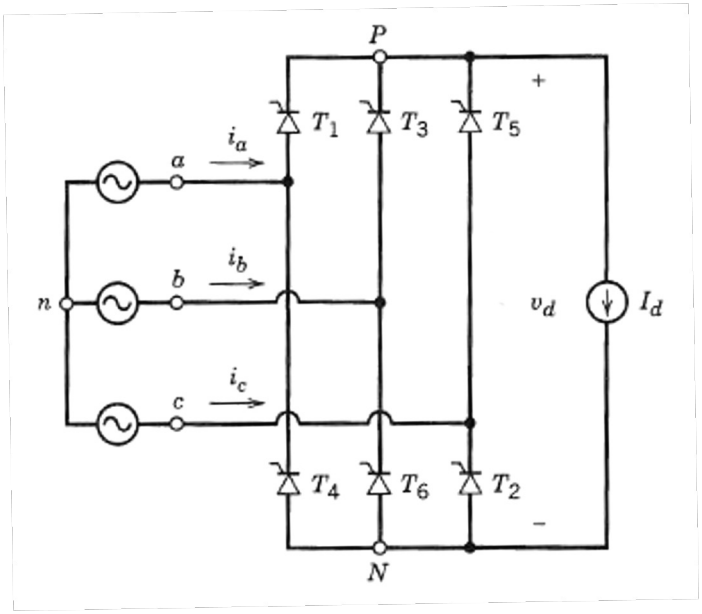


- Secondary current overdamped in snubber after reversal



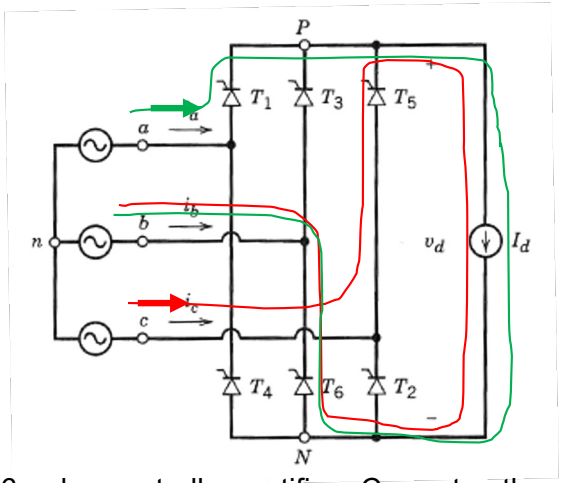
Controlled Rectifier Converters

- Used in higher power applications to rectify the line voltages to create a DC voltage/current source
- Typically use a 3-phase system to feed 6 or 12 thyristors (with a phase shift transformer)
- Begin analysis with idealized circuit and constant current load



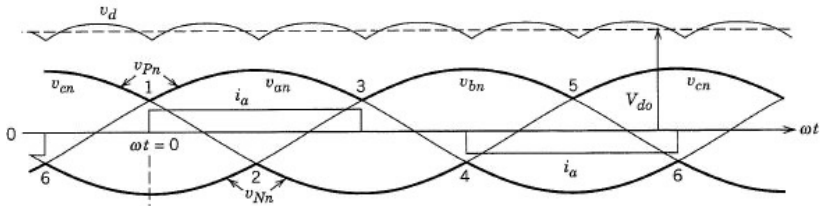
Mohan, N., Undeland, T., and Robbins, W., *Power Electronics Converters, Applications, and Design*, John Wiley and Sons, 1989.

Controlled Rectifier Converters

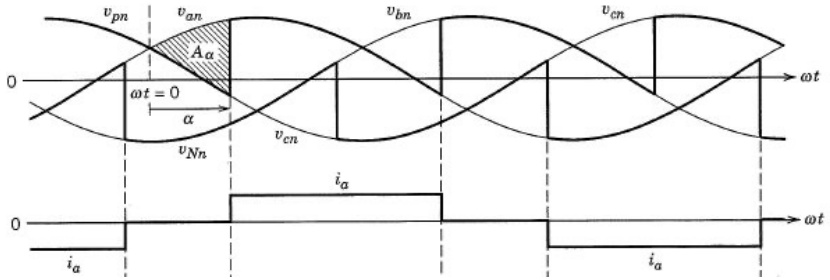


6-pulse controller rectifier. Current path prior to t=0 in red, current path after t=0 in green

- Phase angle α to control DC output
- For converter operation, $0^\circ \leq \alpha \leq 90^\circ$



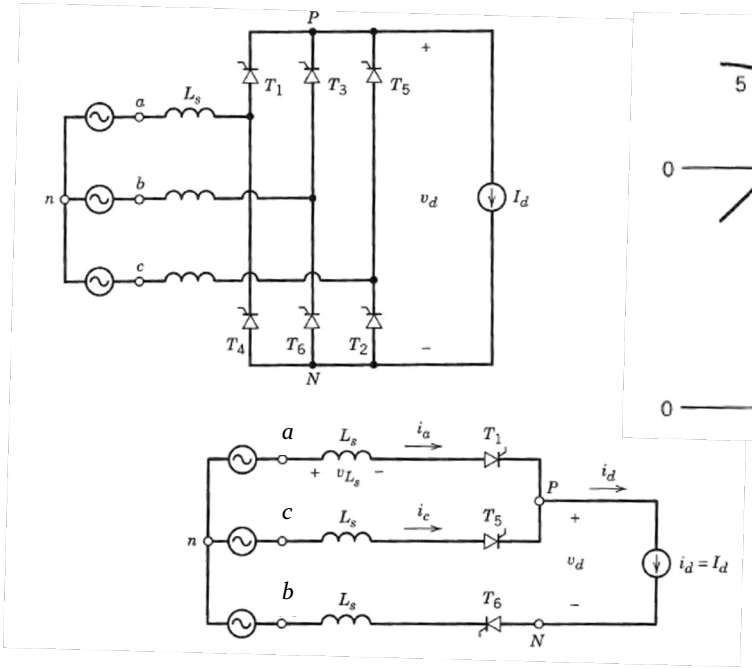
Waveforms for α=0. $V_d = 1.35\ V_{LL}$

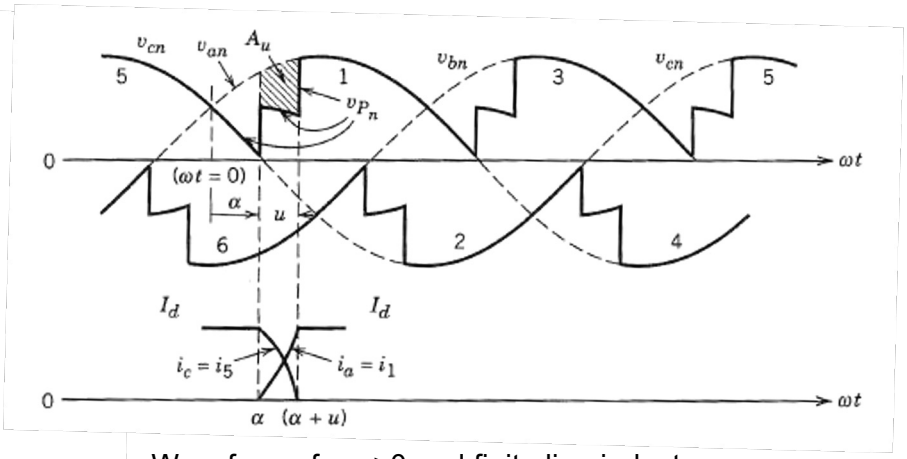


Waveforms for α>0. $V_\alpha = 1.35\ V_{LL} \cos(\alpha)$

Controlled Rectifier Converters with line inductance

- ≥5% AC inductance mandatory in German VDE standards $\omega L_s \geq 0.05\ V_{LL}/(\sqrt{3}\ I_L)$
- AC inductance limits bolted fault currents
- Line side transformers add inductance

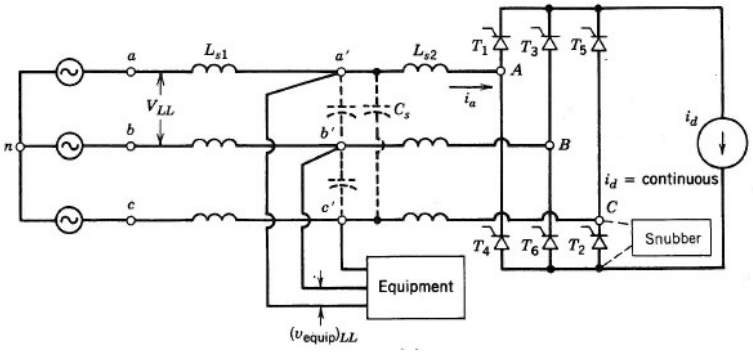


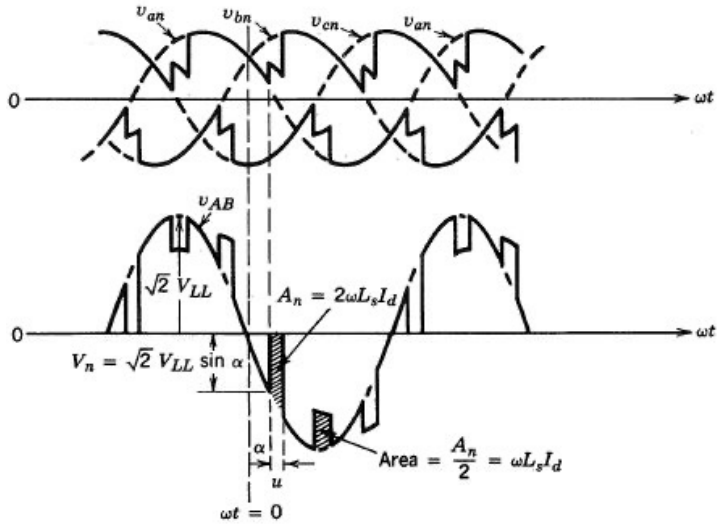


Waveforms for α>0 and finite line inductance.
$V_\delta = 1.35\ V_{LL} \cos(\alpha) - 3\omega L_s I_d/\pi$

Practical considerations for Controlled Rectifier Converters

- Line notching can occur at the point of common coupling (PCC) on an AC distribution system
- This can cause problems with sensitive electronics connected to PCC
- Notch depth at PCC reduced by $L_{s1}/(L_{s1}+L_{s2})$ relative to that at the converter
- For small u, notch width ≈ $2\omega L_s I_d/(\sqrt{2}V_{LL}\sin\alpha)$ radians





Harmonics and power factor on Controlled Rectifier Converters

- Harmonics generated are fundamental and others according to harmonic number:

  h = pn ± 1 where p is the pulse number of the converter and n=1,2,…

- For the 6-pulse system presented, harmonics are 5^{th}, 7^{th}, 11^{th}, 13^{th}, …
- Amplitudes of harmonics are (1/h) that of the fundamental
- Power factor can be derived

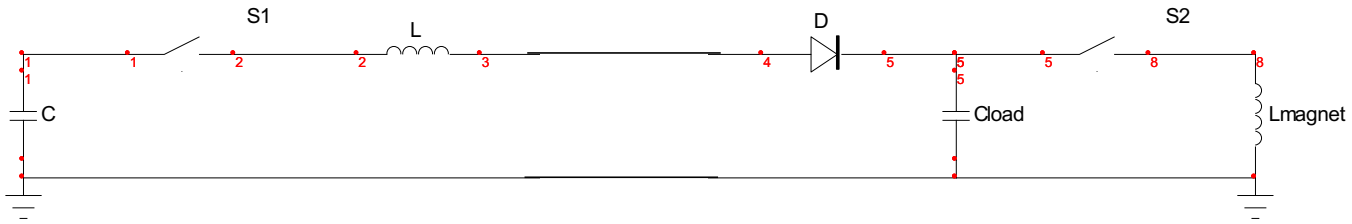
$$PF = (3/\pi)\cos\alpha$$

- IEEE-519 defines harmonic limits at PCC

Maximum Harmonic Current Distortion in Percent of I_L						
Individual Harmonic Order (Odd Harmonics)						
I_{SC}/I_L	<11	11≤*h*<17	17≤*h*<23	23≤*h*<35	35≤*h*	TDD
<20*	4.0	2.0	1.5	0.6	0.3	5.0
20<50	7.0	3.5	2.5	1.0	0.5	8.0
50<100	10.0	4.5	4.0	1.5	0.7	12.0
100<1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0
Even harmonics are limited to 25% of the odd harmonic limits above.						
Current distortions that result in a dc offset, e.g. half-wave converters, are not allowed.						
* All power generation equipment is limited to these values of current distortion, regardless of actual I_{sc}/I_L.						
Where I_{sc} = maximum short-circuit current at PCC. I_L = maximum demand load current (fundamental frequency component) at PCC. TDD = Total demand distortion (RSS), harmonic current distortion in % of maximum demand load current (15 or 30 min demand). PCC = Point of common coupling.						

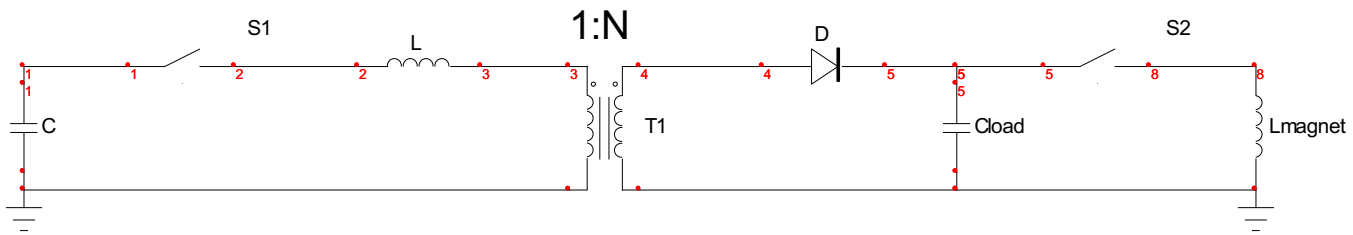
Example

- Design a simple resonant charging system to charge a 100 nF capacitor to 10 kV using a 1 kV capacitor charging supply. This is for an abort kicker system that extracts beam from a storage ring operating at 60 Hz. To ensure that beam is not delivered to the ring prior to the kicker being charged, the 100 nF capacitor must be charged at least 6.7 ms prior to firing the kicker. Assume all circuit elements are ideal. S1 peak current cannot exceed 10 A. Stored energy in the capacitor must not exceed 10 J due to safety concerns. Determine the main component values and maximum switch current to satisfy the design requirements.



- Vmax @ C_{load} = $2V_0(C/(C+C_{load}))$ → $2V_0$ < 10 kV so a transformer is required

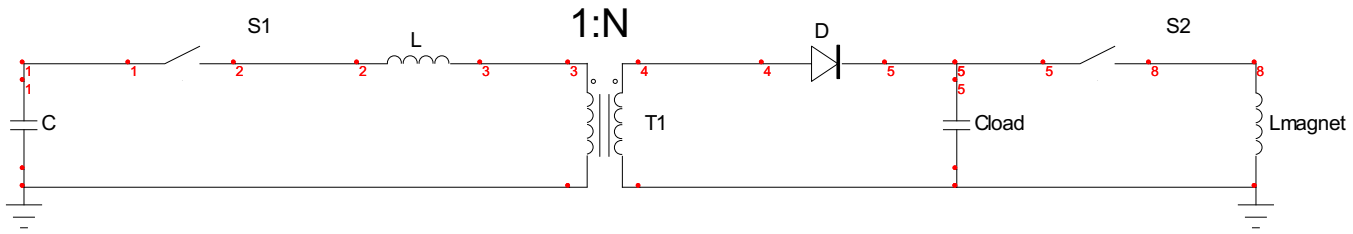
Example



Equations:

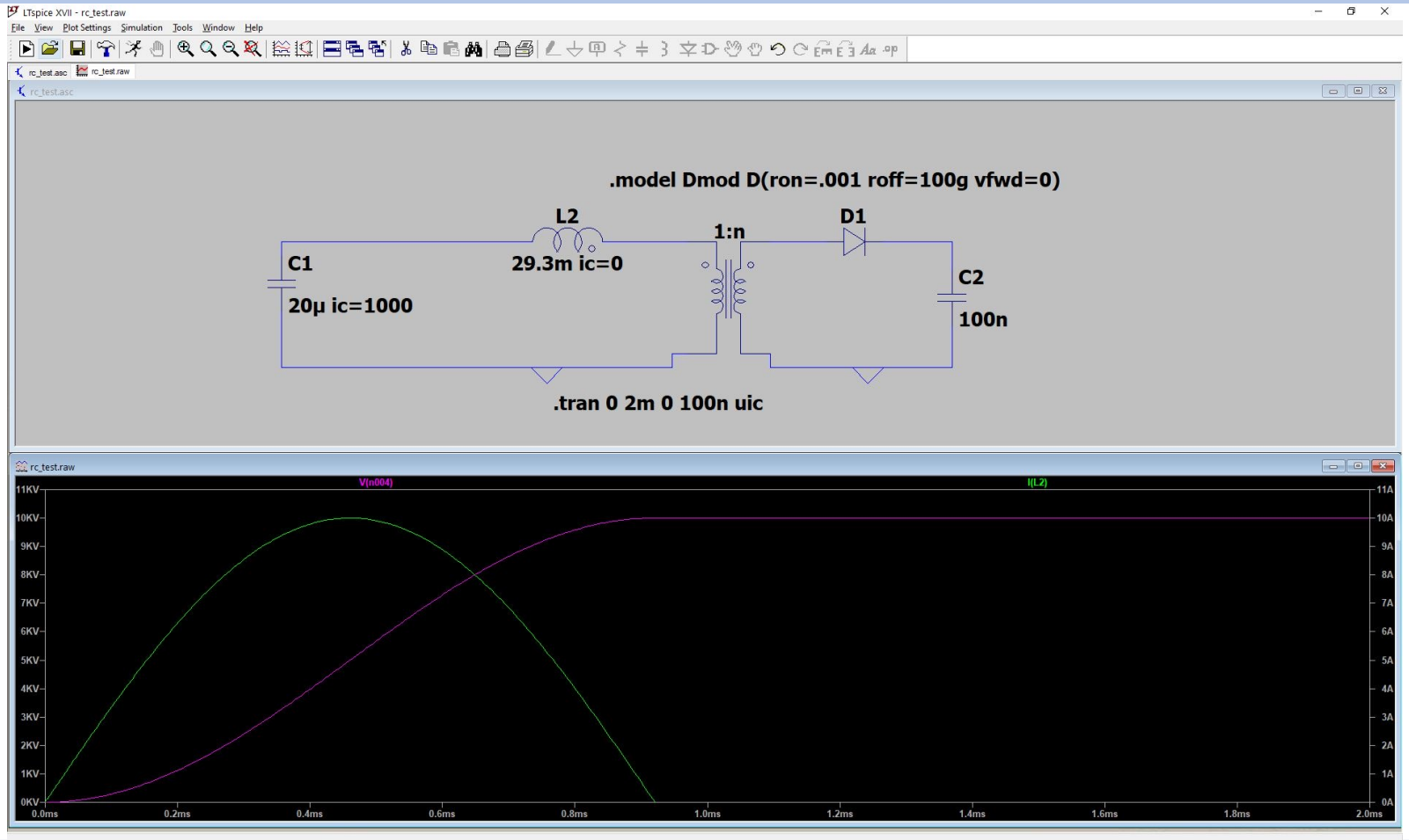
1. $E < 10\ J \rightarrow C \leq 20/V_0^2 = 20\ \mu F$
2. $2N(C/(C+N^2C_{load})) = 10$
3. $N>5$ to achieve desired voltage gain
4. $I_{peak} = V_0(C_{eq}/L)^{1/2} \leq 10$
5. $t_{max} = \pi/\omega = \pi(LC_{eq})^{1/2} \leq (1/60) - 6.7 \times 10^{-3} = 10 \times 10^{-3}$
6. $C_{eq} = N^2CC_{load}/(N^2C_{load}+C)$

Example



- From equation 2, $C = 5N^2C_{load}/(N-5)$. Substituting $C=20\times10^{-6}$ yields $N^2-40N+200 = 0$, or $N = 5.86$, 34.14. Since $N^2C_{load} < C$ for voltage gain, $N < 10$.
- From equation 6, $C_{eq} = 2.93\ \mu F$
- If we set $I_{peak} = 10$ A, $L = 29.3$ mH from equation 4
- Then t_{max} occurs in 920 μs, well within the requirements

Example


LTspice XVII - rc_test.raw
File View Plot Settings Simulation Tools Window Help
rc_test.asc
rc_test.raw
.model Dmod D(ron=.001 roff=100g vfwd=0)
L2
29.3m ic=0
1:n
D1
C1
20µ ic=1000
C2
100n
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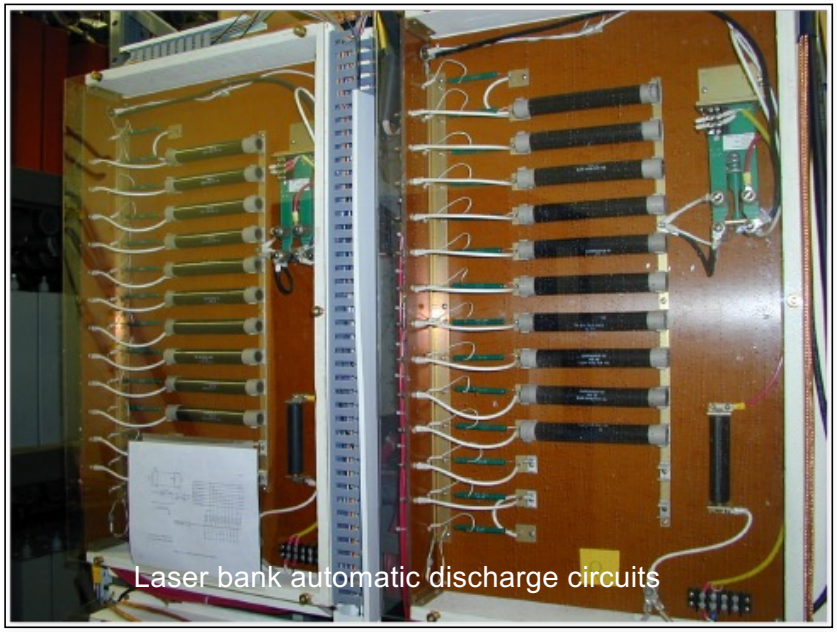
V(n004)
I(L2)
11KV
10KV
9KV
8KV
7KV
6KV
5KV
4KV
3KV
2KV
1KV
0KV
11A
10A
9A
8A
7A
6A
5A
4A
3A
2A
1A
0A
0.0ms
0.2ms
0.4ms
0.6ms
0.8ms
1.0ms
1.2ms
1.4ms
1.6ms
1.8ms
2.0ms

Electrical Safety (ALWAYS CONTACT YOUR AHJ OR SME. THIS IS AN OVERVIEW)

- General electrical hazards are shock and arc flash.
  - Different approach boundaries depending upon AC (power frequencies), DC or AC (radio frequency)
  - Different PPE requirements depending upon voltage, fault energy or electric/magnetic field
  - Two similar standards: DOE Electrical Safety Handbook, DOE_HDBK-1092 & National Electric Code NFPA 70 E
- NFPA 70 E Article 360 deals with capacitors, focus on these, more pulse power unique hazards
- There are shock, thermal / arc flash, hearing, arc blast and lung collapse hazards for capacitors
  - Each hazard has its own keep out boundary and mitigation requirements
- Capacitors as shock hazard
  - (>100 V and >1 J) OR (>400 V and >0.25 J)
- Capacitors as arc flash hazard
  - >100 V and > 10 kJ must review calculation
  - The 1.2 cal/cm^2 limit of category 1 clothing is reached in a box at 44 kJ and 18 inches working distance
- Capacitors as thermal contact burn hazard
  - >100 J, use leather gloves
- Capacitors as an arc blast hazard
  - > 122 kJ there is a lung collapse hazard. This is stated reason remote discharge if > 100 kJ
  - > 1 kJ there is an eardrum rupture hazard at 18”

Electrical Safety (ALWAYS CONTACT YOUR AHJ OR SME. THIS IS AN OVERVIEW)

- High Z (or bleeder) discharge drops voltage to < 100 V and energy to < 5 J
  - < 1000 V wait 3 time constants or 1 minute, which ever is longer
  - > 1000 V time to meet both requirements to be stated.
- Enclosed in protective barrier, conductive preferred
- Visually verifiable wiring integrity highly desired
- Automatic discharge device required when energy stored exceeds 100 kJ
  - Fail safe design and/or redundancy highly desired


Laser bank automatic discharge circuits

Electrical Safety (ALWAYS CONTACT YOUR AHJ OR SME. THIS IS AN OVERVIEW)

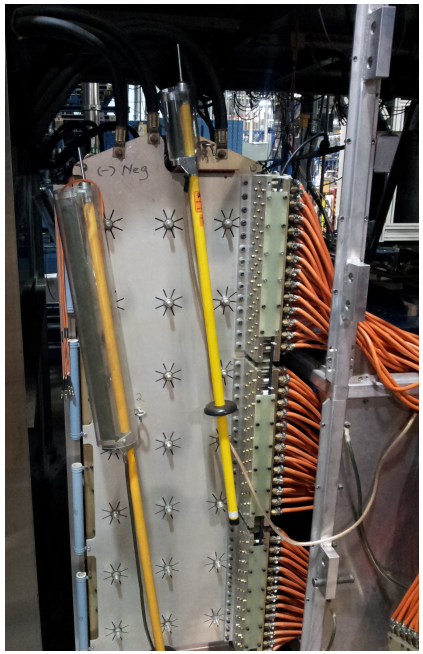
- Some Requirements for >1000 V DC Capacitors from NFPA Article 360, 2021
  Remember shock hazard PPE has different requirements and still applies

Energy	**Stored Energy PPE**	**Energy Discharge & Verification**
0 - 0.25 J	none	Optional
0.25 - 100 J	shock only	Meter or Low Z ground stick
100 J - 1000 J	eyes, ears, thermal + shock	Meter or Low Z ground stick
1 kJ - 100 kJ	eyes, ears, thermal + shock	High Z & Low Z ground stick
> 100 kJ	Same as > 10 kJ, calculate arc blast and lung collapse boundary	Remote High Z & Low Z required

Always visually verify high Z and low Z sticks before use, measure periodically
Always verify meter operation before and after use
Bleeder resistors to reduce voltage to < 100 V & < 5 J within stated time

Electrical Safety

Require multiple grounding sticks for floating capacitors



Capacitor failure can create shrapnel, oil spillage and other hazards requiring special precautions

Diagnostic Techniques and Considerations in Pulsed Power Systems

- Voltage measurement
  - Voltage divider
    - Resistive
    - Capacitive
    - Balanced / Compensated
  - Commercial voltage probes
- Current measurements
  - Current Viewing Resistor (CVR)
  - Rogowski
  - Self-integrating Rogowski
- Grounding
  - Proper grounding
  - Ground loops

Measuring High Voltage

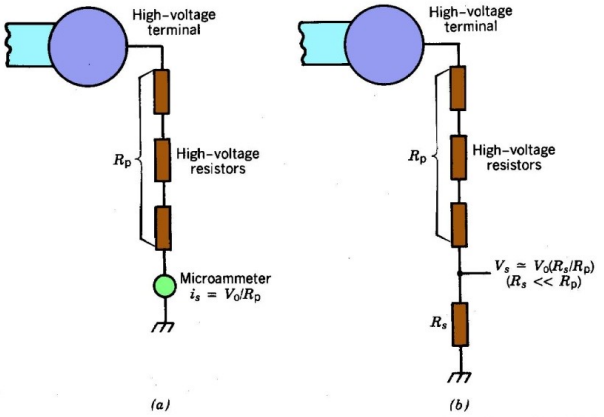


Figure 9.49 High-voltage measurements with resistor strings. (*a*) Resistive shunt. (*b*) Resistive divider.

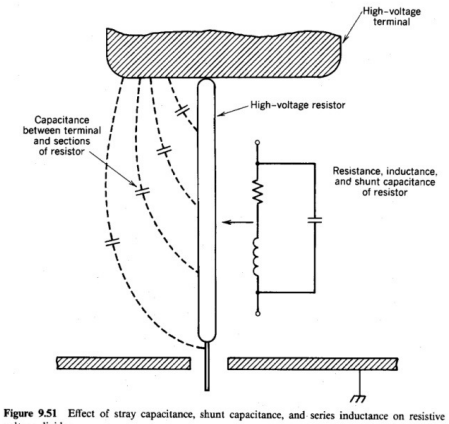


Figure 9.51 Effect of stray capacitance, shunt capacitance, and series inductance on resistive voltage divider.

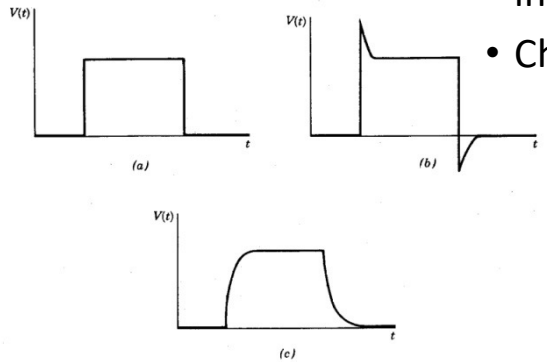
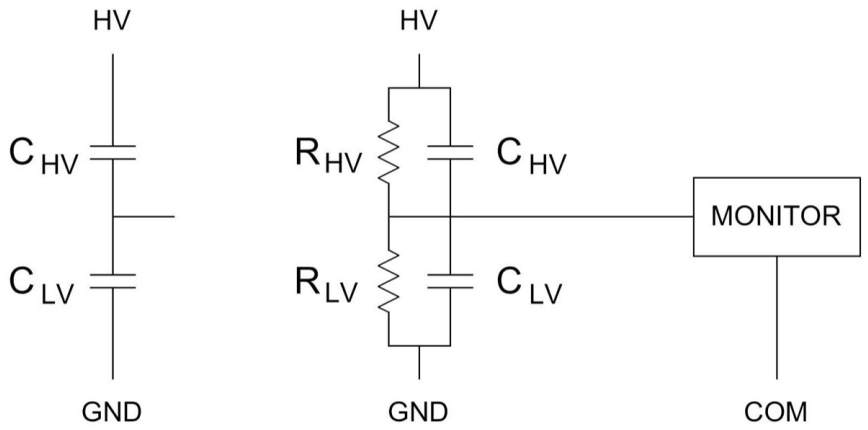


Figure 9.52 Waveforms from resistive voltage divider. (*a*) Ideal output voltage from a square-pulse input. (*b*) Output with significant shunt capacitance. (*c*) Output with significant series inductance.

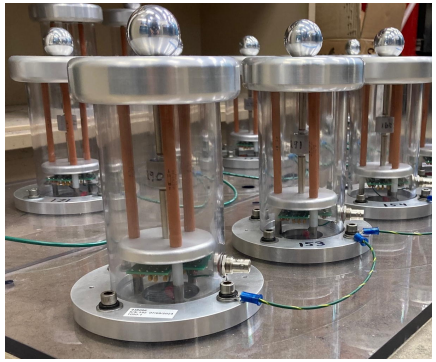
- High voltage resistor strings are used to make HV measurements
  - Resistive shunts
  - Resistive dividers
- Parasitic effects (illustrated in Fig 9.51) can introduce waveform distortion at higher frequencies as illustrated in Fig 9.52
- Impact of parasitic elements is reduced as time constant is reduced, but dissipation and loss increases
- Change to compensated divider if needed

High Frequency Voltage Dividers

- Most common alternatives
  - Capacitive divider – low frequency response can suffer
    - Ratio = C_{HV} / (C_{LV} + C_{HV})
  - Balanced or compensated divider
    - Add capacitance to try to swamp stray capacitance
    - Can be done with discrete components
    - Typical design of commercial HV probes
    - Must take into account loading of monitor
    - Ratio = R_{LV} / (R_{LV} + R_{HV})
    - $R_{LV}C_{LV} = R_{HV}C_{HV}$ for compensated divider
  - Stray capacitance to monitor point will increase C_{HV} and often require empirical tuning



Commercial (Ross Engineering) and Custom

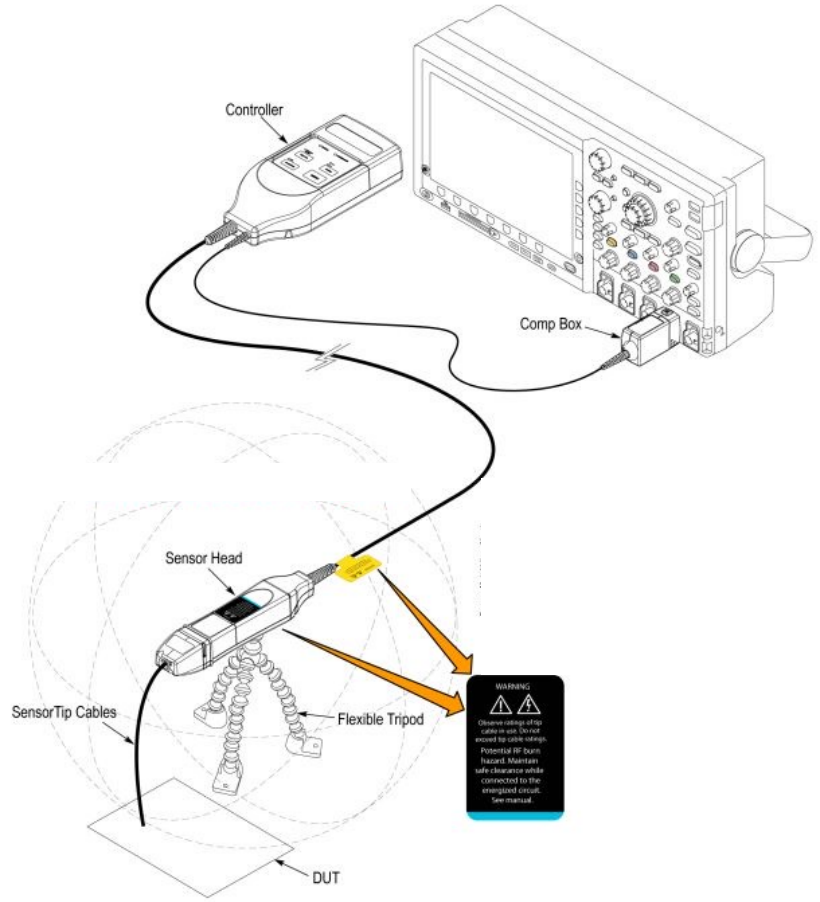


Scope Probes

- Balanced probes
  - Input impedance is frequency dependent
  - Scope impedance impacts response
- Bandwidth is limited
  - May be substantially less than rating, depending on ground connection
- HV versions require tuning to scope
- Pulsed power workhorses
  - P5100: 100X, 2.5 kV, 250 MHz
  - P6015: 1000X, 20 kV, 75 MHz
  - P5210 (differential): 5 kV, 50 MHz, 2 kV common-mode

New Class of probes, Tektronix IsoVue

- Extremely high common mode rejection ratio 160 dB @ DC
- 60 kV common mode voltage isolation
- Up to ±2500 V differential voltage
- Up to 1 GHz analog bandwidth
- Galvanic isolation through fiber optic connection



Current Measurement

- Current viewing resistor
  - V = IR
  - Must keep parasitic inductance time constant small compared to rise time of signal
- Time changing induced magnetic field, dB/dt
  - B-dot loop
    - V = NA dB/dt
      - Coil of area, A, with N turns
    - V = NAB/(RC)
      - Passive RC integrator or use scope integration function, each has tradeoffs
    - Calibration difficult, function of source and loop
      - Location, size and orientation affect measurements
    - Handy for investigations, order of magnitude, shape of response relative to shape of presumed source
  - Rogowski coil – special case of B dot loop
    - Encloses current source
    - Eliminates location/orientation calibration factors

Rogowski Coil

- Usual "air core" approximation, diamagnetic field of loop is negligible
  - Assume $B_i = B$
- $B(r) = \mu I/2\pi\rho$
- $V = NA\, dB/dt$

  $= \mu A(N/2\pi\rho)\, dI/dt$

  $= \mu A(N/\ell)\, dI/dt$

  $= \mu A(N/\ell)I/(RC)$ (with RC integrator)

  ℓ is coil length

  N/ℓ is number of turns/meter
- Can be built in the lab
  - Calibration challenges: accurately measuring A and N/ℓ
  - Signal attenuation from passive RC integrator yields small signals unless I very large or time constant short
- Commercially available

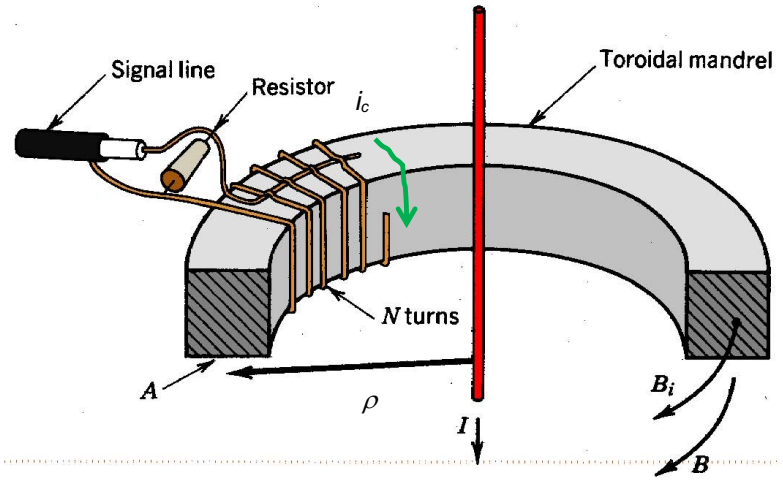


Figure 9.58 Rogowski loop—self-integrating current probe.

Self-integrating Rogowski

- More rigorously, the field B_i, in Fig 9.58

  $B_i = B - \mu\, i_c\, (N/2\pi\rho)$

  where i_c is the current flowing in the coil

  $i_c = NA\, (dB_i/dt)/R$ (1)

- Combining the above and solving for B

  $B = B_i + (dB_i/dt)\, (\mu N^2 A/2\pi\rho R)$

  $= B_i + (dB_i/dt)\, (L/R)$ inserting the identity for a solenoid inductor

- When L/R is large compared to the time scale of current variations

  $(d/dt)\, (L/R) >> 1$, then the left term above can be neglected and:

  $B \approx (dB_i/dt)\, (\mu N^2 A/2\pi\rho R)$

- Recognizing $B = \mu I/2\pi\rho$ and solving for dB_i/dt from (1)

  $i_c = I/(NR)$

- Typically, L is made large by using a ferrite or steel core

Commercial CT
(Pearson, Stangenes & Bergoz)

Grounding

•Universal ground is a fiction, there is always some impedance between any two points and no infinite sink
•Every circuit has a supply and return conductor that should carry normal current
- Ground is a separate conductor for carrying fault current only

•Proper grounding is the single most important factor in making accurate experimental measurements in pulsed power systems: design it in

•kA/μs x nH = V, no two points in a high dI/dt system ever have the same potential which will induce "ground loop" currents

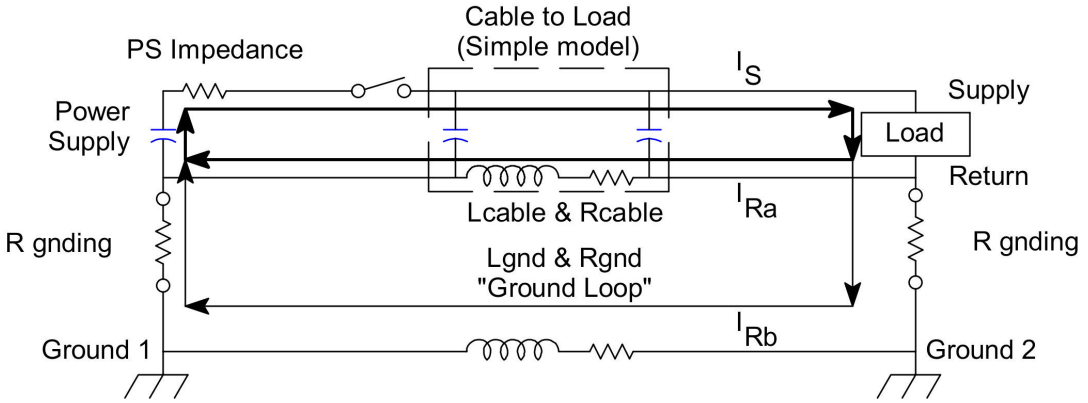
•kA x mOhm of resistance = V, "grounds" which are physically separated by cable resistance will produce "ground loops" for everyone else (*e.g.* beam instrumentation) as well as you

•Solid "earth" ground when possible, low impedance ground to reduce "L"

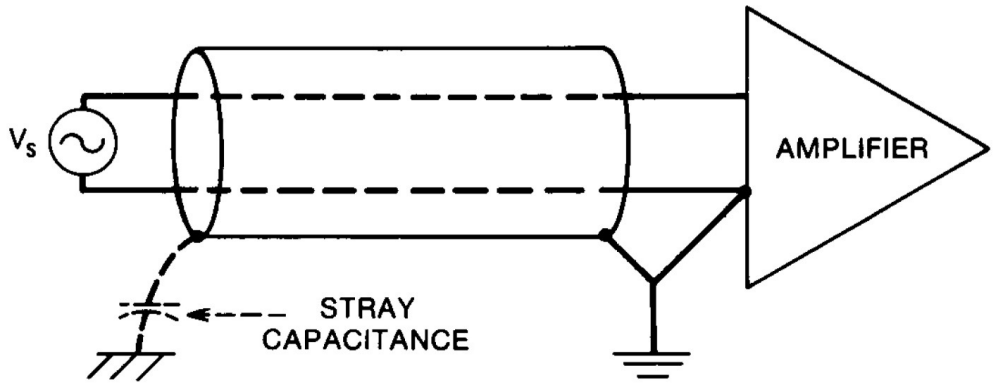
•"Single point" ground systems when possible
- Almost anything with an AC plug has a ground lead
- Safety requirements often result in additional grounds
- Daisy-chained grounds on high di/dt systems can cause problems

Ground Loop

DC coupled

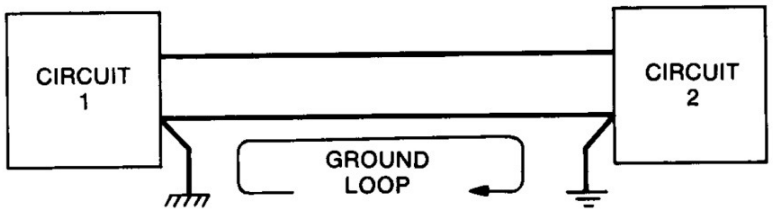


Capacitively coupled

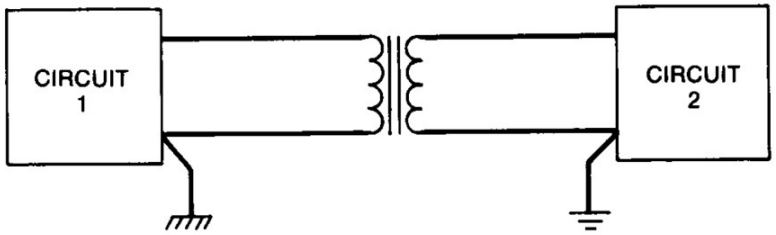


Isolation Techniques for Ground Loops

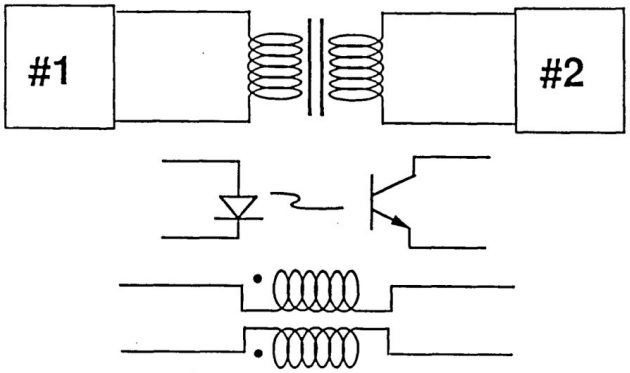
Ground loop from multiple-point grounding



Interrupting ground loop current flow using transformer isolation



Additional isolation techniques

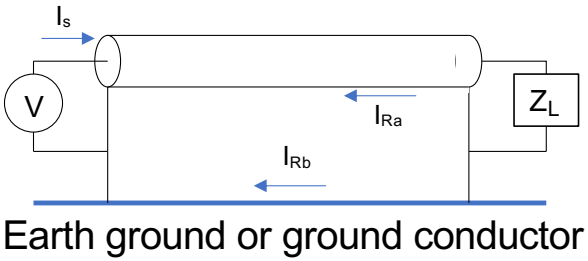


Isolation transformer – unshielded, capacitive coupling will minimize effectiveness at high frequencies, signal droop at low frequencies

Optocoupler – excellent for low-level digital signals but pre- and post-coupler cabling can re-introduce noise, need two power sources, one at each end

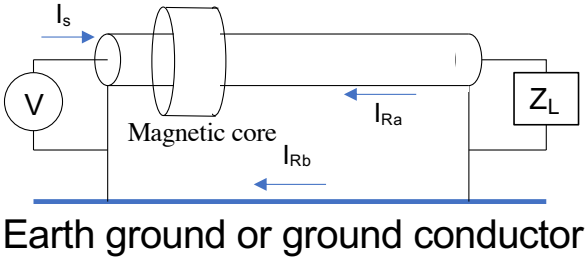
Common-mode choke – effective for common mode at higher frequencies (ωL high), unipolar pulses can result in reduced common mode impedance

Cabling for ground loops



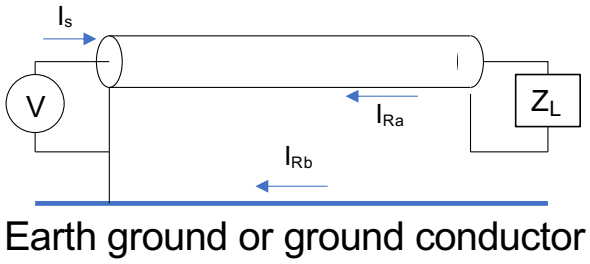
Noise induced as since $I_s \neq I_{Ra}$

Mostly an issue ~kHz frequencies where ground path impedance is low compared to shield



Noise reduced as $I_{Rb} \rightarrow 0$

Ferrite or tape wound steel core increases mutual inductance between center conductor shield increasing inductance of ground path

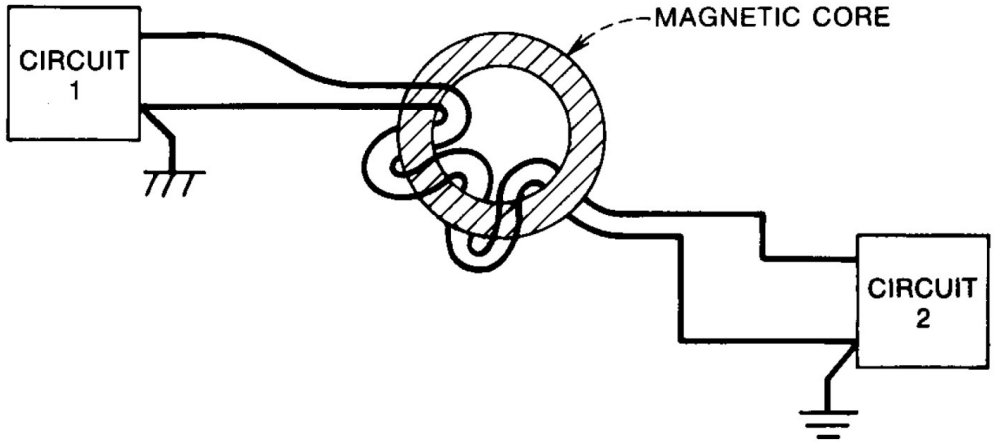


Noise at minimum as $I_{rb} = 0$

Not always feasible to isolate high power loads due to safety or other concerns (capacitance to ground)

Can work for signal (twin-axial cable)

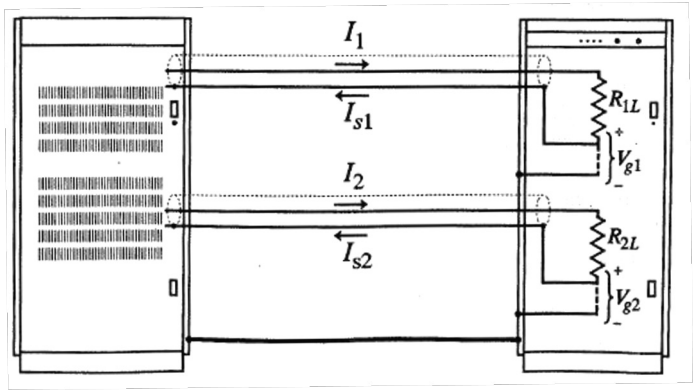
Common Mode Choke for Signal Cables



- Remember discussion of magnetic cores, cut core and small gap for high B_r materials to keep ΔB large, μ higher
- Both examples have same core, same number of coax cable turns, same low frequency impedance
- Better winding has lower capacitance across core, keeps high impedance to higher frequency.

Better Ok

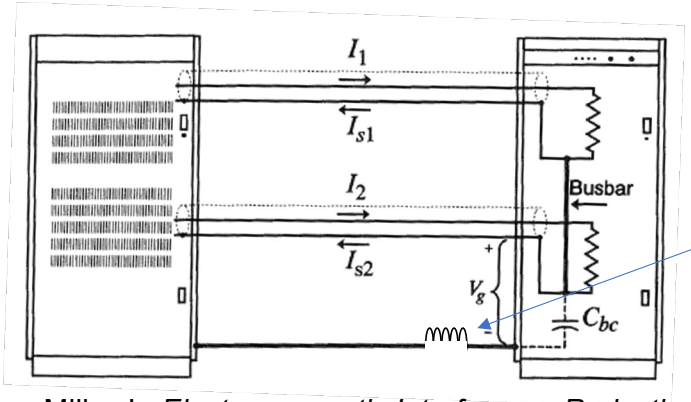
Cabling between equipment



Best to eliminate V_{g1} and V_{g2} connections

If not possible, can use ferrite torroids on signal cables

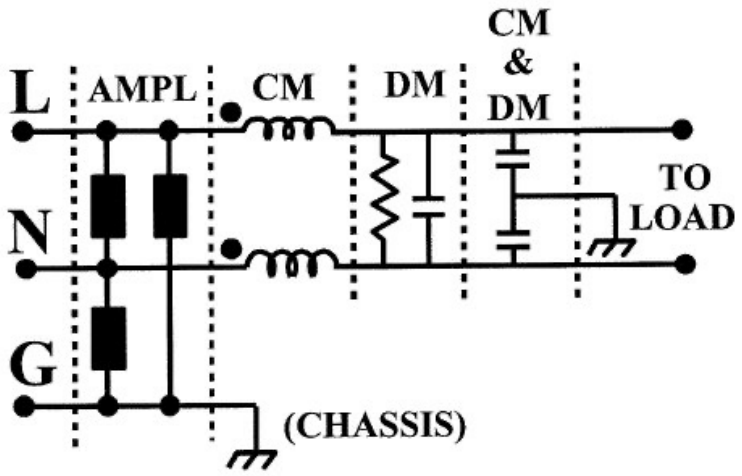
Could isolate load rack, but NEC doesn't permit if AC power present and capacitive coupling to ground may couple high frequency signals



Can add a choke to block high frequency return currents for critical applications

Mills, J., *Electro-magnetic Interference Reduction in Electronic Systems*, PTR Prentice Hall, 1993.

AC Line filtering



- Good line filters employ amplitude-selective, mode-selective and frequency-selective filtering for conducted noise
  - MOV or transorbs to prevent over-voltages
  - Common-mode inductors for common-mode noise
  - High and/or low-pass filters with discrete components
  - Should be used in all chassis designs for pulsed power systems

Control System Functions

- Control output waveform
  - Voltage
  - Pulse shape
  - Timing
- Protect system (MPS)
  - Over voltage
  - Over current
  - Other external interfaces
- Protect personnel (PPS)
  - PPS interlocks
  - Emergency Off
  - Access interlocks
  - Energy discharge
    - Bleeder resistors across capacitors
    - Engineered grounds

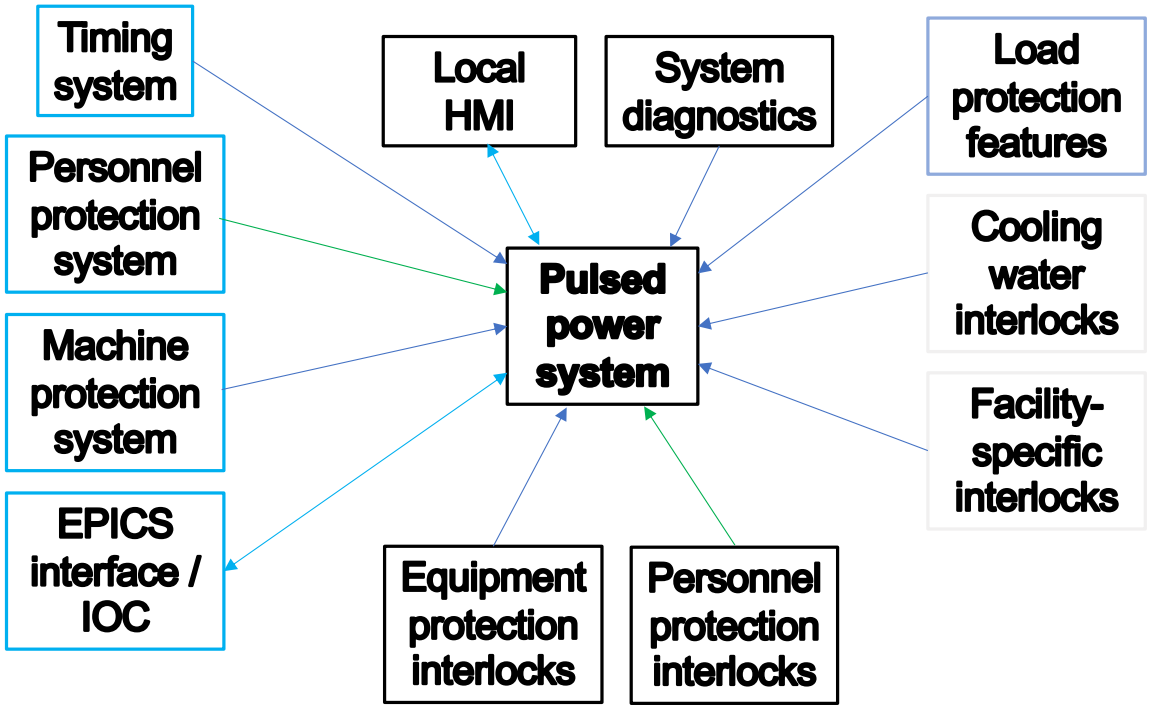
Control System Elements in lab setting

- Lab or prototype scale: independent elements
  - Charging supply with integrated controls
  - Trigger generator
  - Diagnostics
    - Oscilloscope
    - Probes
      - Voltage divider
      - Current transformer
  - System level (e.g. cooling water interlocks)

Control System Elements in facility setting

- Installations
  - Control system interfaces to many operators/users and many other machines/systems: an integrated control system is required
    - Periodic evaluation
    - Software and security updates
    - Configuration control
  - Control system may incorporate many elements at varying levels
    - Integrated modulator control (modern trend)
    - System level (e.g. HPRF)
    - Facility level (e.g. accelerator)

Control System Elements in accelerator complex

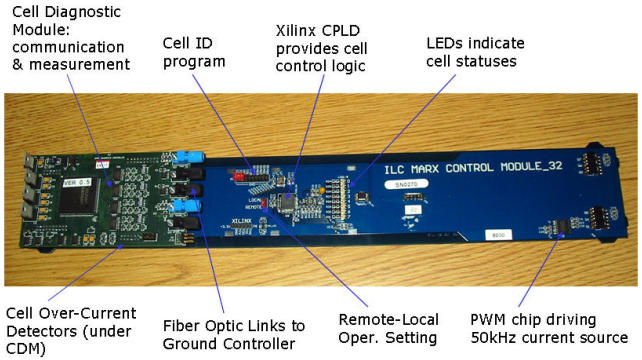


Integrated Control Elements

- Programmable Logic Controller (PLC)
  - Replaces relay logic
  - Serial communication interface (EPICS support)
  - Limitations
    - Slow
    - Loop timing not clocked
    - Expand capabilities with additional circuits
      - Sample-hold
      - Peak detect
      - Various A-D and D-A

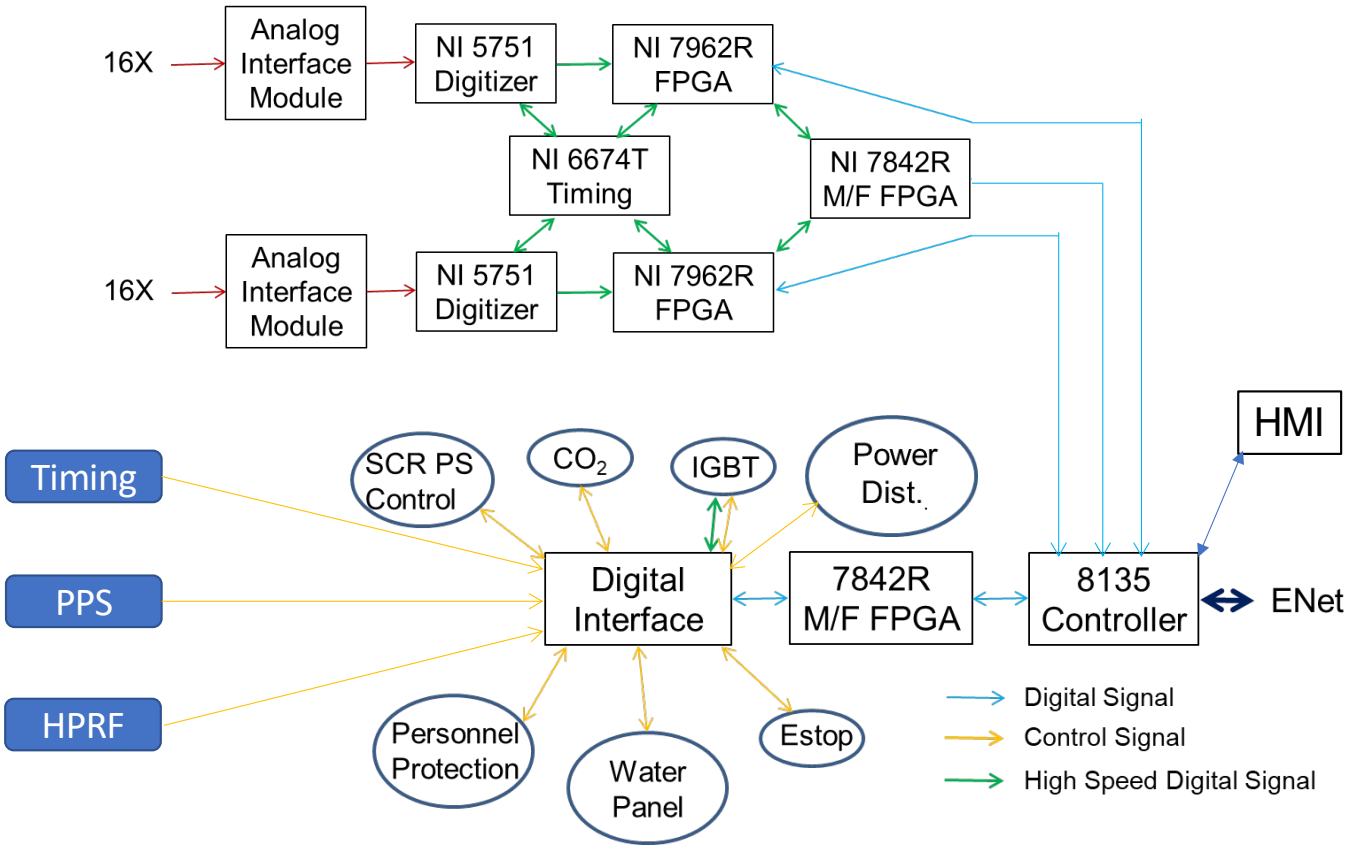
- Programmable logic devices (DSP, FPGA)
  - Fast, to >100 MHz clock
  - Powerful
  - Compact
  - Flexible
  - Communication options
  - Inexpensive (after development costs)

ILC-Marx PLC chassis



Control board for SLAC developed ILC-Marx

Elements of the SNS HVCM controller with CompactRIO FPGA



HMI Options with modern controllers